TRIDENT IoT

T32CZ20

Sub-GHz Z-Wave RF SoC

Description

The T32CZ20 is an ultra-low power, high performance Sub-GHz wireless SoC supporting Z-Wave to facilitate sensor network, building automation, smart locks and smart home applications. It utilizes a fractional-N frequency synthesizer for precise frequency tuning with high resolution, ensuring excellent signal integrity and stability while maintaining power efficiency. This makes the "CZ20" ideal for battery-powered devices and applications where both performance and energy efficiency are essential.

Harnessing the power of ARM Cortex®-M33 and TrustZone technology, the CZ20 SoC establishes secure enclaves to safeguard critical data and processes. The integration of PUFrt®, a Physical Unclonable Function (PUF) based Root of Trust, adds an extra layer of security by leveraging unique physical variations within the chip to generate device-specific cryptographic keys, enhancing resistance to cloning. Complementing these features, the True Random Number Generator (TRNG) ensures the generation of unpredictable and truly random numbers, vital for cryptographic operations and secure communications.

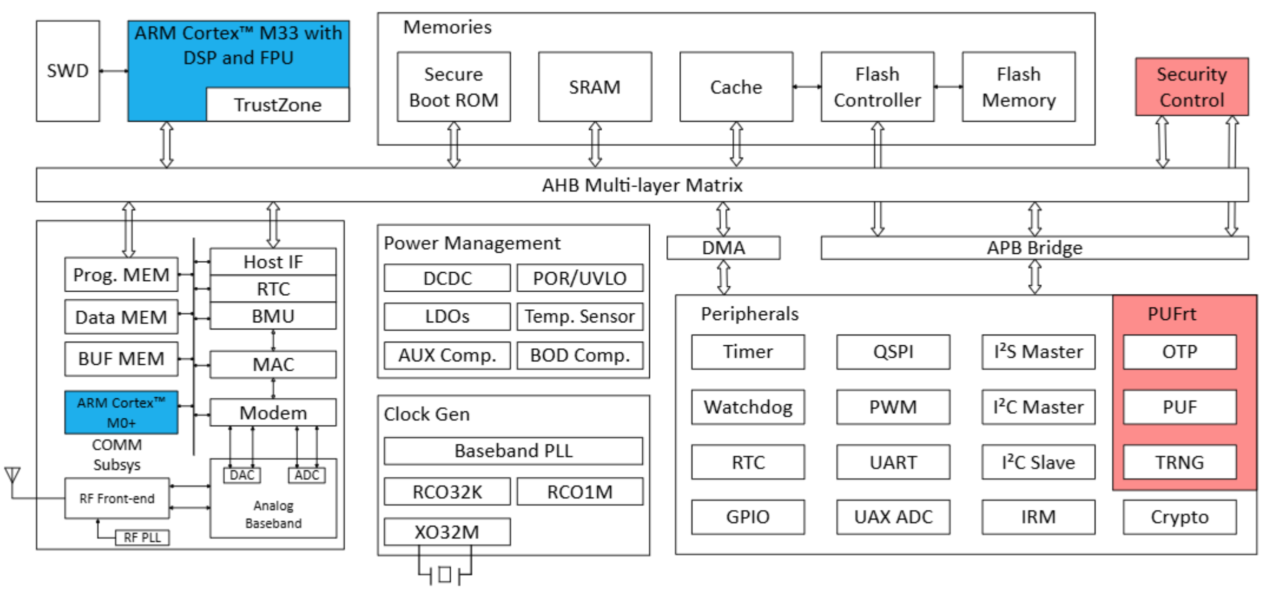


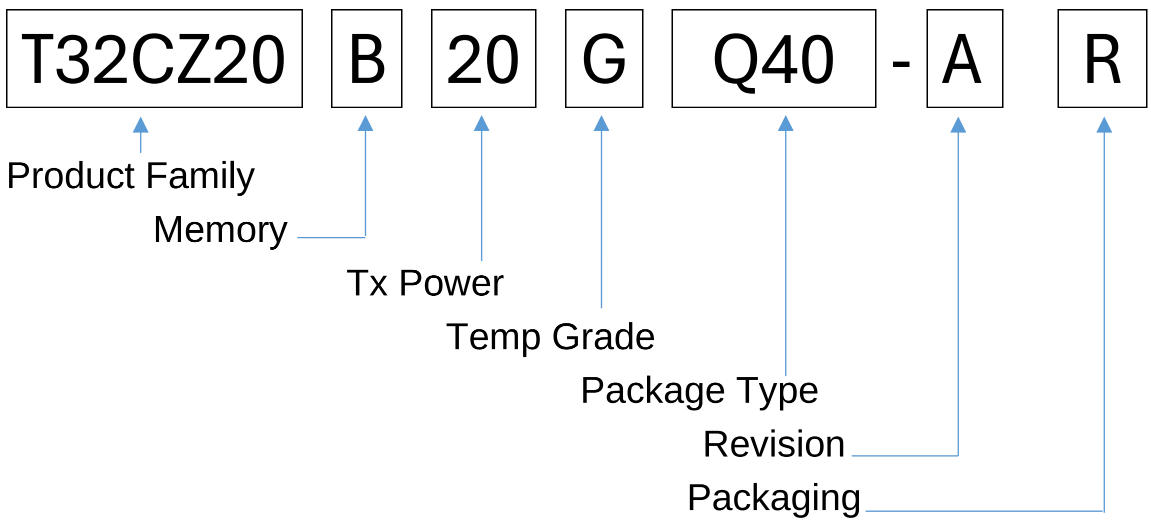
Figure 1 T32CZ20 Block Diagram

Feature List

- Transmit Power
  - 14 dBm @ 1.6 V VDD_PA
  - 20 dBm @ 3.3 V VDD_PA
- Receive Sensitivity
  - -112 dBm @ 9.6 kbps FSK
  - -110 dBm @ 40 kbps FSK
  - -107 dBm @ 100 kbps GFSK
  - -108 dBm @ 100 kbps DSSS O-QPSK
- Fractional-N PLL for precise RF channel tuning
- Supported Modulations
  - (G)FSK with configurable shaping
  - DSSS O-QPSK
- Supported Data Rates
  - 9.6 kbps FSK
  - 40 kbps FSK
  - 100 kbps GFSK
  - 100 kbps DSSS O-QPSK
- Low Power Consumption
  - 5.8 mA RX current
  - 83 mA TX current @ 20 dBm
  - 25 mA TX current @ 14 dBm
  - 4.0 uA in Sleep 1
  - 1.9 uA in Sleep 2
  - 1.2 uA in Deep Sleep
  - 0.5 uA in Deep Power-down
- Operating Range
  - 1.8 V to 3.6 V single supply voltage
  - -40 to +85 °C
- Power Managements
  - Buck DC/DC converter
  - LDO regulators
  - BOD comparator
- SoC System
  - ARM Cortex®-M33 up to 64 MHz with DSP extensions and FPU
  - 288 KB SRAM (192 KB available)
  - 1 MB Flash
- SoC Peripherals
  - DMA
  - Watchdog Timer
  - RTC Timer
  - 32-bit Timer x5
  - PWM x5
  - UART x3 (two with flow control)
  - (Q)SPI x2
  - I^2C Master x2
  - I^2C Slave
  - I^2S Master
  - Infrared Modulator
  - GPIO x22
  - 12-bit, 350 kbps AUX ADC, up to 4 channel
  - AUX Comparator
  - Temperature Sensor
- Security Function
  - Security Control
  - Secure PUF/OTP
  - TRNG
  - Hardware Crypto Engine supporting AES128/192/256, SHA224/SHA256, ECDH/ECDSA, ECJ-PAKE, and Curve25519
- Package
  - 5 mm x 5 mm QFN40
  - Halogen-free
  - Lead-free
  - RoHS 2.0
  - Reach Annex 14 and 17

Ordering Information

Part Number	Package	Shipping	Minimum Order Quantity	Full Carton Quantity
T32CZ20B20GQ40-AR	QFN40 5x5mm	Reel (R)	2,500 pcs	12,500 pcs
T32CZ20B20GQ40-AT	QFN40 5x5mm	Tray (T)	4,900 pcs	29,400 pcs



Field	Values
Product Family	T32CZ20: Wireless Sub-GHz Z-Wave RF SoC
Memory	B = 1024kB
Tx Power	20 = 20dBm
Temp Grade	G = General (-40 to +85C)
Package Type	Q40 = QFN 40
Revision	A = Revision A
Packaging	R = Tape & Reel T = Tray

Pin Assignments

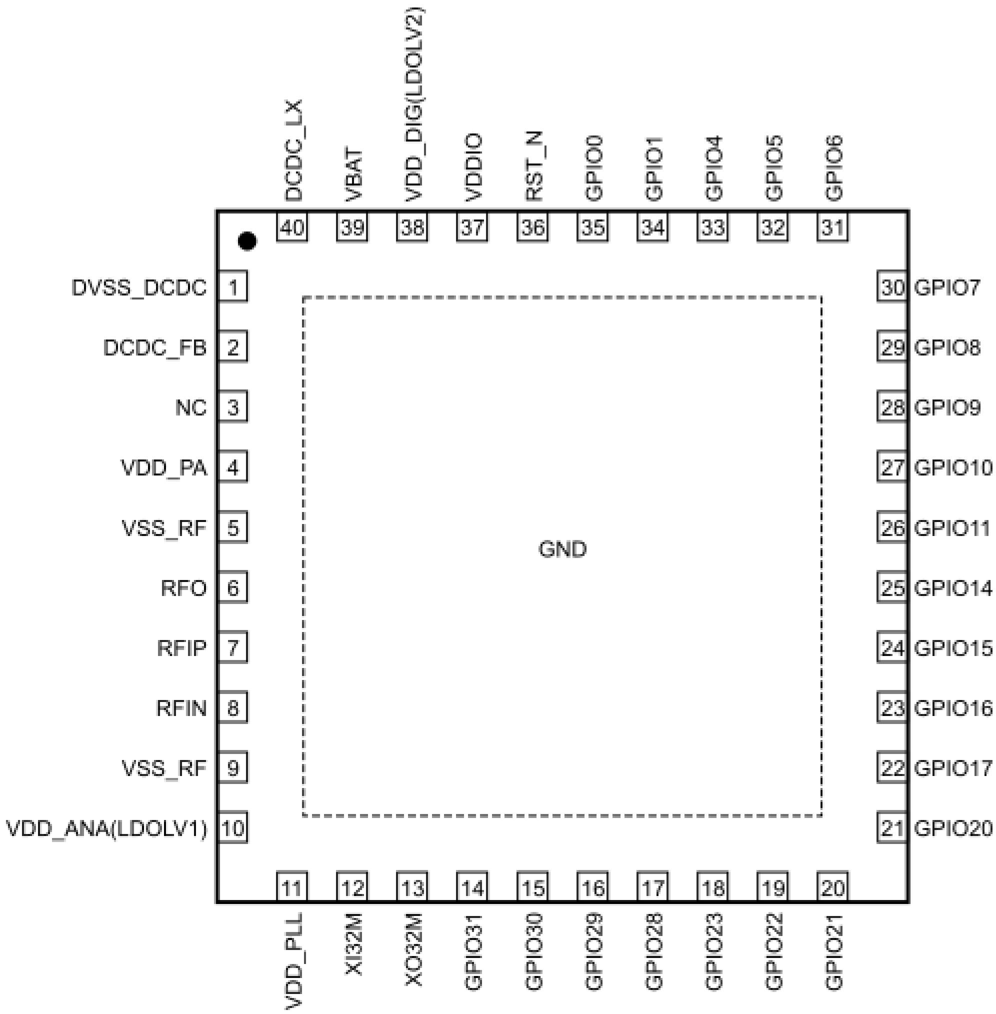


Figure 2 QFN40 Pinout

Table 1 Pin Assignments of QFN40

No.	Pin Name	Type	Description
1	DVSS_DCDC	ground	ground for PMU and DCDC
2	DCDC_FB	power	DCDC feedback input
3	NC		not connected
4	VDD_PA	power	supply for PA
5	VSS_RF	ground	ground for RF
6	RFo	RF	Sub-GHz RF output
7	RFIP	RF	Sub-GHz RF differential input P
8	RFIN	RF	Sub-GHz RF differential input N

No.	Pin Name	Type	Description
9	VSS_RF	ground	ground for RF
10	VDD_ANA(LDOLV1)	power	supply for Analog / LDOLV1 output
11	VDD_PLL	power	supply for RF PLL
12	XI32M	analog	32MHz crystal oscillator
13	XO32M	analog	32MHz crystal oscillator
14	GPIO31	DIO	multi-function digital I/O
15	GPIO30	DIO	multi-function digital I/O
16	GPIO29	DIO	multi-function digital I/O
17	GPIO28	DIO	multi-function digital I/O
18	GPIO23	DIO	multi-function digital I/O
19	GPIO22	DIO	multi-function digital I/O
20	GPIO21	DIO	multi-function digital I/O
21	GPIO20	DIO	multi-function digital I/O
22	GPIO17	DIO	multi-function digital I/O, default UART0_TX
23	GPIO16	DIO	multi-function digital I/O, default UART0_RX
24	GPIO15	DIO	multi-function digital I/O
25	GPIO14	DIO	multi-function digital I/O
26	GPIO11	DIO	multi-function digital I/O, default ARM MCU ICE data
27	GPIO10	DIO	multi-function digital I/O, default ARM MCU ICE clock
28	GPIO9	DIO	multi-function digital I/O
29	GPIO8	DIO	multi-function digital I/O
30	GPIO7	DIO	multi-function digital I/O
31	GPIO6	DIO	multi-function digital I/O
32	GPIO5	DIO	multi-function digital I/O
33	GPIO4	DIO	multi-function digital I/O
34	GPIO1	DIO	multi-function digital I/O
35	GPIO0	DIO	multi-function digital I/O
36	RST_N	DI	external reset input
37	VDD_IO	power	supply for GPIO
38	VDD_DIG(LDOLV2)	power	supply for Digital / LDOLV2 output
39	VBAT	power	supply for PMU
40	DCDC_LX	power	DCDC filter

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System Overview

Introduction

The T32CZ20 is an ultra-low power, high performance ARM® Cortex®-M33 based RF SoC supporting various protocol stacks to facilitate home & building automation, smart lighting, smart locks, sensor network, etc. applications. Designed with efficiency in mind, the "CZ20" boasts low power consumption, ensuring extended battery life for seamless operation. Its compact size and robust connectivity make it an ideal choice for integrating into a variety of devices.

Harnessing the power of ARM Cortex®-M33 and TrustZone technology, CZ20 establishes secure enclaves to safeguard critical data and processes. The integration of PUFrt®, a Physical Unclonable Function (PUF) based Root of Trust, adds an extra layer of security by leveraging unique physical variations within the chip to generate device-specific cryptographic keys, enhancing resistance to cloning. Complementing these features, the True Random Number Generator (TRNG) ensures the generation of unpredictable and truly random numbers, vital for cryptographic operations and secure communications.

SoC CPU

The Cortex®-M33 CPU is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- outstanding processing performance combined with fast interrupt handling
- efficient processor core, system and memories
- ultra-low power consumption with integrated sleep modes
- platform security robustness with TrustZone

Table 2 Configurable Options of Cortex®-M33 in T32CZ20

Core Option	Description	Implementation
FPU	Floating Point Unit	YES
DSP	DSP Extension	YES
SECEXT	Security Extension	YES
SAU	Security Attribution Unit	YES (Use platform-defined security control unit instead)
NUMIRQ	Number of IRQ inputs	48
IRQLVL	Control bits of IRQ priority level	3 (8 levels)
DBGLVL	Debug level	2 (Full set of debug resources)
ITM	Instrumentation Trace Macrocell	No
ETM	Embedded Trace Macrocell	No
MTB	Micro Trace Buffer	No
WIC	Wake-up Interrupt Controller	Yes
Endianness	Memory system endianness	Little endian
JTAG/SWD	Debug interface	SWD only

Memory Map

Table 3 Memory Map

Modules	Size	Non-secure Address	Secure Address
Flash	128MB	0x00000000~0x07FFFFFF	0x10000000~0x17FFFFFF
Boot ROM	32KB	N/A	0x18000000~0x18007FFF
Reserved		0x08008000~0x0FFFFFFF	0x18008000~0x1FFFFFFF
RAM 0	32KB	0x20000000~0x20007FFF	0x30000000~0x30007FFF
RAM 1	32KB	0x20008000~0x2000FFFF	0x30008000~0x3000FFFF
RAM 2	32KB	0x20010000~0x20017FFF	0x30010000~0x30017FFF
RAM 3	32KB	0x20018000~0x2001FFFF	0x30018000~0x3001FFFF
RAM 4	32KB	0x20020000~0x20027FFF	0x30020000~0x30027FFF
RAM 5	16KB	0x20028000~0x2002BFFF	0x30028000~0x3002BFFF
RAM 6	16KB	0x2002C000~0x2002FFFF	0x3002C000~0x3002FFFF
Reserved		0x20030000~0x2003FFFF	0x30030000~0x3003FFFF
COMM Subsys RAM	96KB	0x20040000~0x20057FFF	0x30040000~0x30057FFF
Reserved		0x20030000~0x2FFFFFFF	0x30030000~0x3FFFFFFF
System Control	4KB	0x40000000~0x40000FFF	0x50000000~0x50000FFF
GPIO Control	4KB	0x40001000~0x40001FFF	0x50001000~0x50001FFF
Reserved		0x40002000~0x40002FFF	0x50002000~0x50002FFF
Security Control	4KB	N/A	0x50003000~0x50003FFF
RTC Timer	4KB	0x40004000~0x40004FFF	0x50004000~0x50004FFF
Deep Power-down Control	4KB	0x40005000~0x40005FFF	0x50005000~0x50005FFF
Power Management	4KB	0x40006000~0x40006FFF	0x50006000~0x50006FFF
Reserved		0x40007000~0x40007FFF	0x50007000~0x50007FFF
Reserved		0x40008000~0x40008FFF	0x50008000~0x50008FFF
Flash Control	4KB	0x40009000~0x40009FFF	0x50009000~0x50009FFF
Timer 0	4KB	0x4000A000~0x4000AFFF	0x5000A000~0x5000AFFF
Timer 1	4KB	0x4000B000~0x4000BFFF	0x5000B000~0x5000BFFF
Timer 2	4KB	0x4000C000~0x4000CFFF	0x5000C000~0x5000CFFF
Slow-clock Timer 0	4KB	0x4000D000~0x4000DFFF	0x5000D000~0x5000DFFF
Slow-clock Timer 1	4KB	0x4000E000~0x4000EFFF	0x5000E000~0x5000EFFF
Reserved		0x4000F000~0x4000FFFF	0x5000F000~0x5000FFFF
Watchdog Timer	4KB	0x40010000~0x40010FFF	0x50010000~0x50010FFF
Reserved		0x40011000~0x40011FFF	0x50011000~0x50011FFF
UART 0	4KB	0x40012000~0x40012FFF	0x50012000~0x50012FFF
UART 1	4KB	0x40013000~0x40013FFF	0x50013000~0x50013FFF
Reserved		0x40014000~0x40014FFF	0x50014000~0x50014FFF

Modules	Size	Non-secure Address	Secure Address
Reserved		0x40015000~0x40015FFF	0x50015000~0x50015FFF
Reserved		0x40016000~0x40016FFF	0x50016000~0x50016FFF
Reserved		0x40017000~0x40017FFF	0x50017000~0x50017FFF
I2C Slave	4KB	0x40018000~0x40018FFF	0x50018000~0x50018FFF
Reserved		0x40019000~0x40019FFF	0x50019000~0x50019FFF
COMM Subsys	4KB	0x4001A000~0x4001AFFF	0x5001A000~0x5001AFFF
Reserved		0x4001B000~0x4001BFFF	0x5001B000~0x5001BFFF
Reserved		0x4001C000~0x4001CFFF	0x5001C000~0x5001CFFF
BOD Comparator	4KB	0x4001D000~0x4001DFFF	0x5001D000~0x5001DFFF
AUX Comparator	4KB	0x4001E000~0x4001EFFF	0x5001E000~0x5001EFFF
Reserved		0x4001F000~0x4001FFFF	0x5001F000~0x5001FFFF
QSPI 0	4KB	0x40020000~0x40020FFF	0x50020000~0x50020FFF
QSPI 1	4KB	0x40021000~0x40021FFF	0x50021000~0x50021FFF
Reserved		0x40022000~0x40022FFF	0x50022000~0x50022FFF
Reserved		0x40023000~0x40023FFF	0x50023000~0x50023FFF
IRM	4KB	0x40024000~0x40024FFF	0x50024000~0x50024FFF
UART 2	4KB	0x40025000~0x40025FFF	0x50025000~0x50025FFF
PWM	4KB	0x40026000~0x40026FFF	0x50026000~0x50026FFF
Reserved		0x40027000~0x40027FFF	0x50027000~0x50027FFF
xDMA	4KB	0x40028000~0x40028FFF	0x50028000~0x50028FFF
DMA 0	4KB	0x40029000~0x40029FFF	0x50029000~0x50029FFF
DMA 1	4KB	0x4002A000~0x4002AFFF	0x5002A000~0x5002AFFF
I2C Master 0	4KB	0x4002B000~0x4002BFFF	0x5002B000~0x5002BFFF
I2C Master 1	4KB	0x4002C000~0x4002CFFF	0x5002C000~0x5002CFFF
I2S	4KB	0x4002D000~0x4002DFFF	0x5002D000~0x5002DFFF
Reserved		0x4002E000~0x4002EFFF	0x5002E000~0x5002EFFF
AUX ADC	4KB	0x4002F000~0x4002FFFF	0x5002F000~0x5002FFFF
Software IRQ 0	4KB	0x40030000~0x40030FFF	0x50030000~0x50030FFF
Software IRQ 1	4KB	0x40031000~0x40031FFF	0x50031000~0x50031FFF
Reserved		0x40032000~0x4043FFFF	0x50032000~0x5043FFFF
PUFrt	32KB	0x40044000~0x40047FFF	0x50044000~0x50047FFF
Crypto Engine	16KB	0x60000000~0x60003FFF	0x70000000~0x70003FFF

Clocks

There are several clock sources in CZ20 and they are summarized in Table 4.

Table 4 Clock Sources in T32CZ20

Clock Name	Type	Typical Frequency	Comment
xtal_clk	Crystal oscillator	32 MHz	The default clock for SoC CPU, memories and peripherals.
pll_clk	PLL	36/40/48/64 MHz	A higher frequency clock for SoC CPU and memories.
rco32k	RC oscillator	32 kHz	The default clock for slow-clock timers.

The 32 MHz Crystal Oscillator

Since CZ20 is a SoC chip for wireless communications, a crystal oscillator of 32 MHz (xtal_clk) is required for establishing communication links correctly. It is also the default clock for SoC CPU, memories and peripherals after power on.

The Baseband PLL

The Baseband PLL (pll_clk) provides a higher clock frequency than 32MHz that can boost the performance of SoC CPU and memories. Available clock options of the Baseband PLL are 36, 40, 48, and 64 MHz.

The 32 kHz RC Oscillator

The 32 kHz RC oscillator (rco32k) is used for slow-clock timers, like RTC timer and slow-clock Timers. The rco32k is kept power-on in Sleep Mode but is powered off in Deep Sleep Mode by default.

A divided-by-2 option is supported for the rco32k that can further reduce the power consumption in low power modes.

Resets

The reset sources and their targets of CZ20 are summarized in Table 5 and graphically illustrated in Figure 3.

Table 5 Reset Sources and Targets

Reset Source	Type	Signal	Targets		
			Deep Power-down Control	RTC GPIO	All Others
VBAT	Power	vbat_por_n	O	O	O
RST_N	External pin	ext_rst_n	O	O	O
VDD_DIG	Power	vdig_por_n		O	O
Deep power-down wakeup reset	Internal event	dpd_rst_n		O	O
Deep Sleep wakeup reset	Internal event	ds_rst_n			O
Watchdog reset	Internal event	wdt_rst_n			O
Software reset	Internal event	soft_rst_n			O
MCU lockup	Internal event	mcu_lockup_n			O

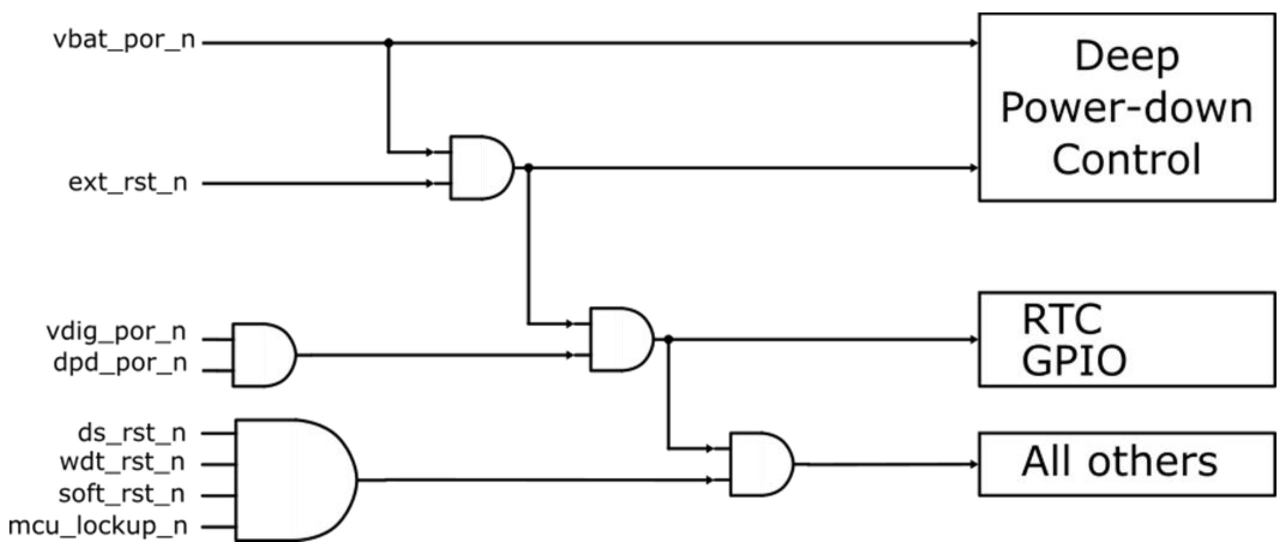

Figure 3 Reset Scheme

Power-on Reset

The power-on reset, vbat_por_n, is triggered when the power source, VBAT, is above the pre-defined threshold. It has the highest priority over other reset signals and will reset the whole system as illustrated in Figure 3.

External Reset

There is a low-actively external reset pin, RST_N, that can reset the whole chip externally. To active the external reset, RST_N shall be asserted for at least 100us. A 100K ohm pull-up resistor is attached to the RST_N pin internally so RST_N can be left floating if not used.

Deep Power-down Wakeup Reset

During Deep Power-down mode, the whole chip is powered off except the Deep Power-down Control. After waking up from the Deep Power-down mode, the reset signal, dpd_rst_n, will be triggered to reset the whole chip.

Deep Sleep Wakeup Reset

During Deep Sleep mode, most of the digital parts are powered off to reduce the leakage current. To let the digital circuits work correctly after waking up from Deep Sleep, a Deep Sleep wakeup reset signal, ds_rst_n, is generated automatically by the hardware to reset the corresponding digital circuits.

Watchdog Reset

When Watchdog Timer is not kicked for a certain period, the watchdog reset is triggered.

Software Reset

The software reset is triggered when the SYSRESETREQ bit in AIRCR register of Cortex-M33 is set. Please refer to the documents of Cortex-M33 for how to set SYSRESETREQ.

MCU Lookup

The Cortex-M33 enters a lockup state if a fault occurs when it cannot be serviced or escalated. In this situation, the processor does not execute any instructions and asserts the LOCKUP signal. It will then trigger the hardware controller to reset the entire the system.

Security Control

With the rapid growth and spread of IoT applications, security is becoming increasingly important. It is necessary to protect valuable data and store it securely. It is also important to prevent unauthorized access.

With the TrustZone technology of Cortex®-M33 and the assistance of specific hardware, CZ20 can provide several levels of security. Due to the limit function of the SAU (Security Attribution Unit) of Cortex®-M33, it should be disabled and use the Security Controller instead.

The security controller controls the security attributes of Flash, RAM and peripherals. Both Flash and RAM can be partitioned into secure, non-secure callable (NSC), and non-secure (NS) regions. Every peripheral can also be set as secure or non-secure. Because Boot ROM is the root of trust, it is always secure.

Crypto Engine

CZ20 incorporates a hardware-based crypto engine that supports various modern cryptography schemes. With the help of Hardware Accelerator, code size, memory size, and execution time for a cryptographic operation is drastically reduced. It also has the benefit of reducing the loading SoC CPU and hence save the power.

The crypto engine supports following cryptographic schemes:

- AES
  - 128-bit, 192-bit and 256-bit key length encryption/decryption
  - ECB, CBC, CTR, CMAC, CCM cipher modes
- SHA224/256
  - Can be extended to HMAC, HMAC DRBG or other
- ECC
  - 192-bit and 256-bit key length
  - Both prime field GF(p) and binary field GF(2m)
  - NIST P-192 curve (also knowns as SECP192R1)
  - NIST P-256 curve (also knowns as SECP256R1 or Prime256v1)
  - NIST B-163 curve (also knowns as SECT163R2)
  - Curve 25519
  - ECDH/ECDSA
  - ECJ-PAKE

PUFRt

T32CZ20 incorporates PUFrt® from PUFsecurity Corp. PUFrt® (Root-of-Trust) is a PUF-based (Physical-Unclonable-Function) secure macro which offers the essential features required for establishing a secure Hardware Root of Trust, including a TRNG, UID and Secure OTP.

PUF

Based on NeoFUF® technology, the PUF has the near ideal characteristics of 50% HW (Hamming-Weight), 50% Inter-HD (Hamming-Distance), 0% Intra-ID HD and 0ppm BER (Bit-Error-Rate). It is able to be used for generating true random bits, which can act as a silicon fingerprint. NeoFUF® passes the

NIST SP800-22 and NIST SP800-90B IID statistical analysis test suites.

Due to the inherent randomness and uniqueness of the PUF, it can be used directly as a Unique Identifier (UID) and/or a Hardware Unique Key (HUK). Additionally, it can serve as the seed for any key derivation function (KDF) to generate a HUK.

OTP

The PUFrt contains two OTPs, labeled OTP1 and OTP2. Each OTP has a total size of 1K bytes, divided into 256 words: otp1_000 to otp1_255 for OTP1 and otp2_000 to otp2_255 for OTP2. Each OTP word is protected by ECC to ensure data integrity. As a result, programming the OTP requires writing the entire word, and byte-level writes are not permitted. Any unprogrammed OTP word will return 0x0 when read.

TRNG

The true random number generator of PUFrt® compliant with NIST SP800-90B recommendations. It is equipped with a digital noise source based on four independent ring oscillators, entropy health tests, and an entropy conditioning engine that is based on a PUF-based algorithm.

Communication Subsystem

The communication subsystem (COMM Subsys) is a tiny but powerful system which is optimized for handling wireless communications. It incorporates an ARM Cortex®-M0+ MCU, a hardware MAC, a Modem, and a RF transceiver that can support multiple wireless communication protocols. With the total 112 KB memory, it is possible to implement multiple protocols in a single firmware and maintain several communication links at the same time.

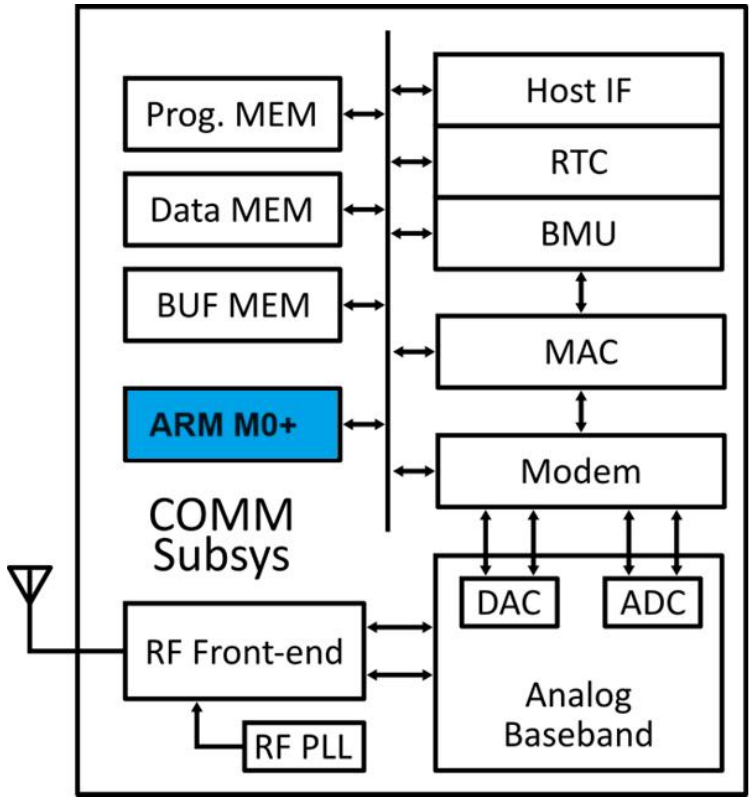

Figure 4 Block Diagram of COMM Subsys

Cortex M0+ MCU

The Cortex M0+ MCU serves as the radio controller and is the core component of the COMM Subsystem. It manages the time-sensitive tasks associated with wireless protocols, schedules transmission and reception timing windows, and handles Listen Before Talk (LBT). This offloads the SoC CPU, freeing up resources for user applications, and significantly reduces power consumption.

Buffer Memory

The COMM Subsystem features an 8K-byte buffer memory for storing transmission and reception packets. This memory is managed by the Buffer Management Unit (BMU) and is organized into multiple queues, supporting one RX queue and up to seven TX queues. The buffer memory is shared by all queues, with a single queue capable of holding up to 4K bytes max. This design offers significant flexibility, making it suitable for supporting a variety of communication protocols.

Host Interface

The Host CPU communicates and exchanges data with the COMM Subsystem through the Host Interface. This interface includes a DMA, a Host Command register, and various status registers, with interrupt functionality also available.

The DMA acts as a bus master, capable of issuing memory read or write transactions in the background. It can generate an interrupt request to the Host CPU once the transaction is complete. There are two types of DMA operations: memory transactions and I/O transactions.

DMA

The DMA is intended to be used as a controller to transfer data directly from memory space to another memory space, including system memories and peripheral devices.

Once configured and enabled, the DMA controller manages data flow from an AHB Master write port bus to another AHB Master read port bus, and initiates data transfers across the two AHB bus through the DMA Buffer.

There are two identical DMA controllers, DMA 0 and DMA 1 in CZ20, that can operate independently.

Software IRQ

Besides the built-in software interrupts of Cortex®-M33, CZ20 provides two additional software interrupts, Software IRQ 0 and Software IRQ 1. Each software interrupt has 32 status bits and one additional data register that can exchange information between software tasks.

Timer

The Timer module is a 32-bit up/down counter with a selectable and programmable pre-scaler whose value can be set between 1 and 1024. The pre-scaler extends the timer's range at the expense of precision.

The Timer provides two modes of operation: free running counting and periodic counting. One-shot counting function is also supported for a single time counting and stopping the timer.

For supporting PWM application in low power mode, the Timer provides simple PWM (pulse-width modulation) function. Timer counts to generate waveform based on the threshold and phase register setting.

Input signal time counting is supported in the Timer. Timer captures the counting value temperately when input signal positive or negative edges.

The Timer contains several configuration registers that can be written and read by the processor. A 10-

bit pre-scaler precedes a 32-bit timer counter. The counter value can be loaded from a preload register. The timer interrupt can be enabled and check the status by the control registers.

Slow-clock Timer

The Slow-clock Timer is a timer running in the rco32k domain. Because rco32k is still active in low-power modes, the Slow-clock Timer can be operated in low-power modes normally and can become the wakeup source. With the interrupt repeat function, it is possible to support the very long sleep time.

Watchdog Timer

Watchdog Timer is very common in current system to prevent some unexpected condition happen to hang the whole system. The Watchdog Timer is a down counting timer which can trigger the system reset and reset the hung system. The Watchdog Timer need to be "kick" periodic to reload the counting value, or system will be reset when the Watchdog Timer count to 0.

This module implements a 32-bit down counter with selectable or programmable pre-scaler to produce a watchdog reset signal, as well as a warning interrupt. The reset and interrupt can be enabled separately.

The Watchdog Timer also supports the Windowing feature. This feature makes the watchdog timer not only have to be kicked in a certain period, but also that can't be kicked too frequently. This mechanism protects the system can be reset when stuck in an always kicking situation.

RTC Timer

The RTC (Real Time Clock) timer provides the calendar function and maintains accurate date and time information. It enables the device to keep track of the current time and date, day of the week, month, and year, represented in a BCD format, which is a binary encoding for decimal numbers. It also allows the system to keep track of time for various functions such as scheduling tasks, time-stamping events, coordinating communication protocols, and maintaining accurate time for applications like alarms, timers, and logging.

GPIO Control

The GPIO control module enables manual control of the CZ20 GPIOs. Each GPIO can be set to input or output mode. In output mode, the SoC CPU can set the output to high or low. In input mode, interrupts can be triggered on the rising edge, falling edge, or both. All GPIOs can be configured as wakeup sources in low-power modes.

UART

The UART module supports Universal Asynchronous Receiver/Transmitter protocol. The data of transmit and receive paths is connected to FIFOs. The core converts bytes into serial bits for transmission, and vice versa. The MCU can access data through FIFOs directly or through DMA controller. Flow control with CTSn/RTSn is also supported.

Table 6 UART Supported Baud Rate

UART Supported Baud Rate (bps)	
2400	115200
4800	230400
9600	460800
14400	500000
19200	576000
28800	921600
38400	1000000
57600	1152000
76800	2000000

QSPI

The Quad Serial Peripheral Interface module either controls a serial data link as a master or reacts to a serial data link as a slave.

The core operates in various data modes (8-bit, 16-bit or 32-bit). The data is serialized and then transmitted, either LSB or MSB first, using the standard 4-wire SPI bus interface or the Quad mode bus.

PWM

The PWM module generates pulse width modulated signals and drives the assigned GPIOs. It supports a pulse generator with up or up-and-down counting modes. Five PWM modules can provide up to 5 PWM channels and each channel have its own individual frequency control. A DMA control is embedded in the PWM module to transfer frequency control between memory and the PWM module without CPU intervention.

I^2C Master

The I^2C Master interface provides supports for the communications link between integrated circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D and D/A converters, CODECs, and many types of microprocessors.

I^2C Master supports the following features:

- Clock synchronization
- 7-bit addressing
- Transmit (9x16) and receive (8x16) buffers
- Interrupt or polling mode operation

I^2C Slave

The I^2C Slave interface is a simple two-wire bus with a software-defined protocol for system control. This circuit is designed for single byte process of transmission/reception and need software to interfere during every byte.

The I^2C Slave supports those features:

- Clock stretching
- 7-bit addressing
- Interrupt or polling mode operation

I^2S

The I^2S is the most common interface to exchange audio data between chips. The I^2S interface of CZ20 supports various sample rates and data formats which is applicable to most applications. It also supports the DMA function to transfer audio samples between memory and the I^2S module without CPU intervention.

The I^2S interface supports those features:

- Support master mode only
- Support MCLK

- Support I2S, Left Justified (LJ), and Right Justified (RJ) formats
- Support 8, 16, 32 and 48 kHz sample rates
- Support 16, 24 or 32-bit data length

IRM

The infrared remote, simple and low-cost technology is very often used in today's homes. The controller provides several of the most frequently used infrared protocols. It is a dedicated peripheral that allows the generation of infrared waveforms for transmitting infrared signals with minimal software overheads.

AUX ADC

The AUX ADC is a successive approximation (SAR) analog to digital converter. It can be used to measure voltages from external analog inputs (AIOs) or from the internal signals like the temperature sensor and the battery. The AIOs are shared with GPIOs and can be configured as single or differential inputs to the AUX ADC. Various sampling modes are provided and the DMA mode is also supported.

AUX Comparator

The AUX Comparator is an analog comparator that compares two voltages, the input voltage V_{in} and the reference voltage V_{ref}. The comparator will output a logical high if V_{in} is greater than V_{ref}, otherwise it will output a logical low. Both input and reference voltages can be selected among AIOs and can be used to monitor the external analog signal.

BOD Comparator

The BOD Comparator is dedicatedly used as the brown-out detector. It is similar to the AUX Comparator but its two inputs are fixed to the divided VDD and the bandgap reference.

Power Management

Power Structure and Connection

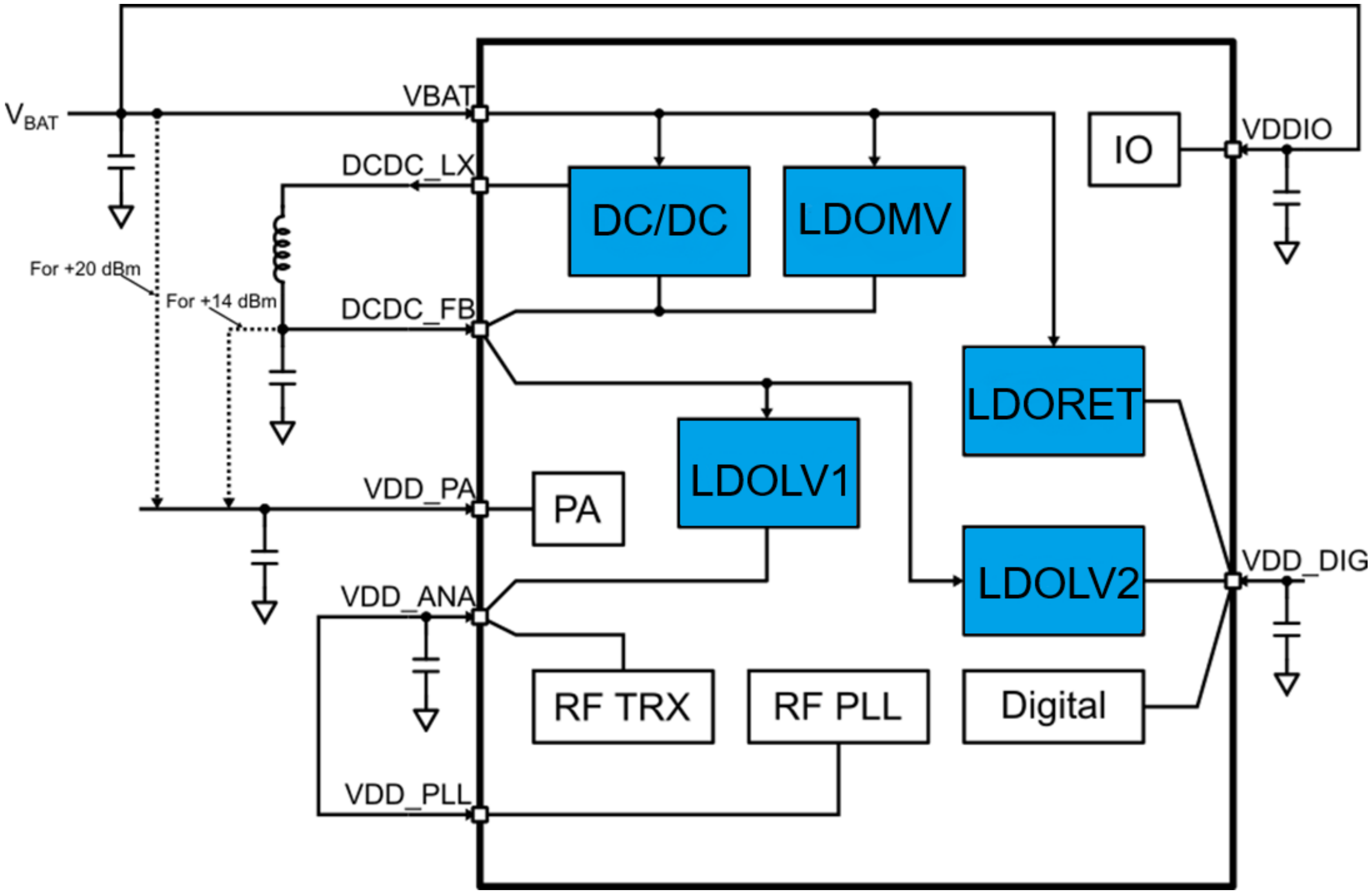

Figure 5 The Power Structure of T32CZ20

The power management contains one DC/DC Buck converter and several LDO regulators. The power structure and the power connection is illustrated in Figure 5.

Powered by V_{BAT} through the VBAT pin, the DC/DC and the LDOMV are at the first level of the power hierarchy. Either one of them will be used but not both and it will then provide the power to the next level LDO regulators, LDOLV1 and LDOLV2. Through internal and external connections, RF and analog circuits (RF TRX and RF PLL) are powered LDOLV1 and the digital circuits (Digital) are powered by LDOLV2. After power-on reset, LDOMV is turned on and DC/DC is turned off by default. Users can switch between LDOMV and DC/DC through the software API.

The transmitter power amplifier (PA) is powered by the pin, VDD_PA. For the +14 dBm output power application, it shall be connected to DCDC_FB while for the +20 dBm one, it shall be powered by V_{BAT} directly.

The retention LDO, LDORET, is used to keep the data and states in low-power modes and all other power management components will be turned off to save the power.

Power-on Sequence

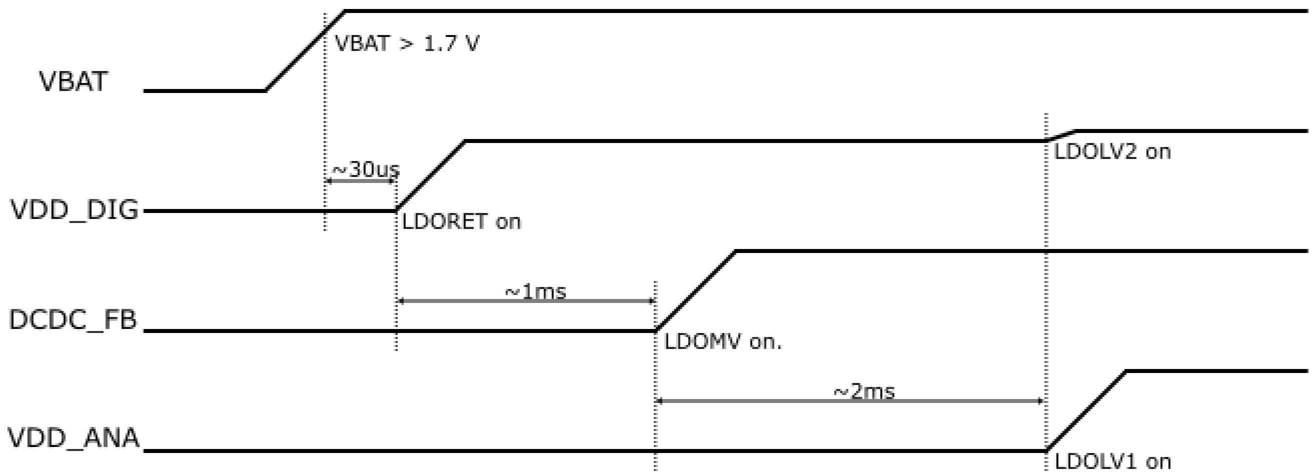

Figure 6 Power-on Sequence

Radio

Antenna Interface

The sub-GHz antenna interface of CZ20 consists of a single-ended output pin (RFO) and differential input pins (RFIP, RFIN). An external balun is required to convert the single-ended signal to a differential input. The RF matching network includes a low-pass filter designed to suppress transmitter harmonics, ensuring compliance with regulatory spectral emission limits and improving overall transmission efficiency. Proper PCB layout and impedance control are essential to minimize losses and maximize RF performance. For example, the RF trace should be kept as short as possible while ensuring it maintains a 50-ohm impedance to ensure signal integrity and reduce potential signal reflections.

RF Matching

The reference RF matching network starting values for +20 dBm output power to a SMA antenna are shown in Figure 7-1.

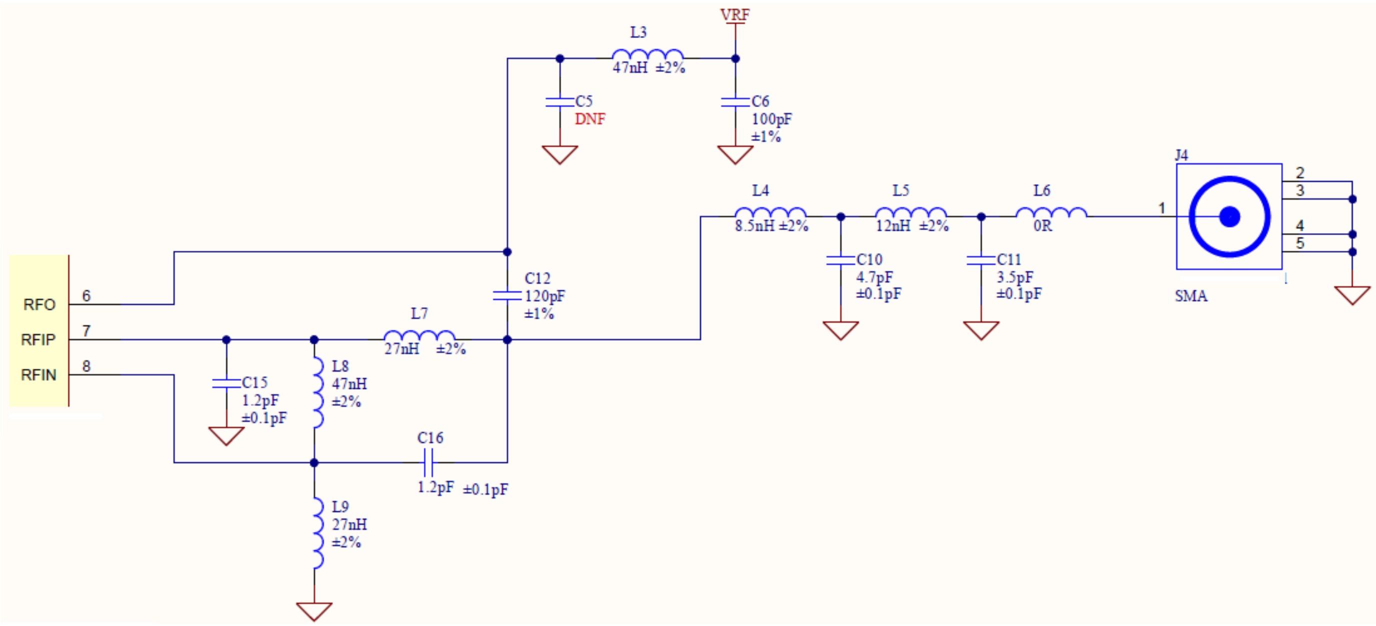

Figure 7-1 Reference RF Matching Network for +20 dBm Output Power

Table 7-1 Component Value of the +20 dBm RF Matching Network

Label	Component Value
L3, L8	47 nH ±2%
L7, L9	27 nH ±2%
L4	8.5 nH ±2%
L5	12 nH ±2%
C15, C16	1.2 pF ±0.1pF
C12	120 pF ±1%
C6	100 pF ±1%
C10	4.7 pF ±0.1pF
C11	3.5 pF ±0.1pF
L6	0 ohm resistor
C5	DNF

The reference RF matching network starting values for +20 dBm output power to a PCB Trace antenna power are shown in Figure 7-2.

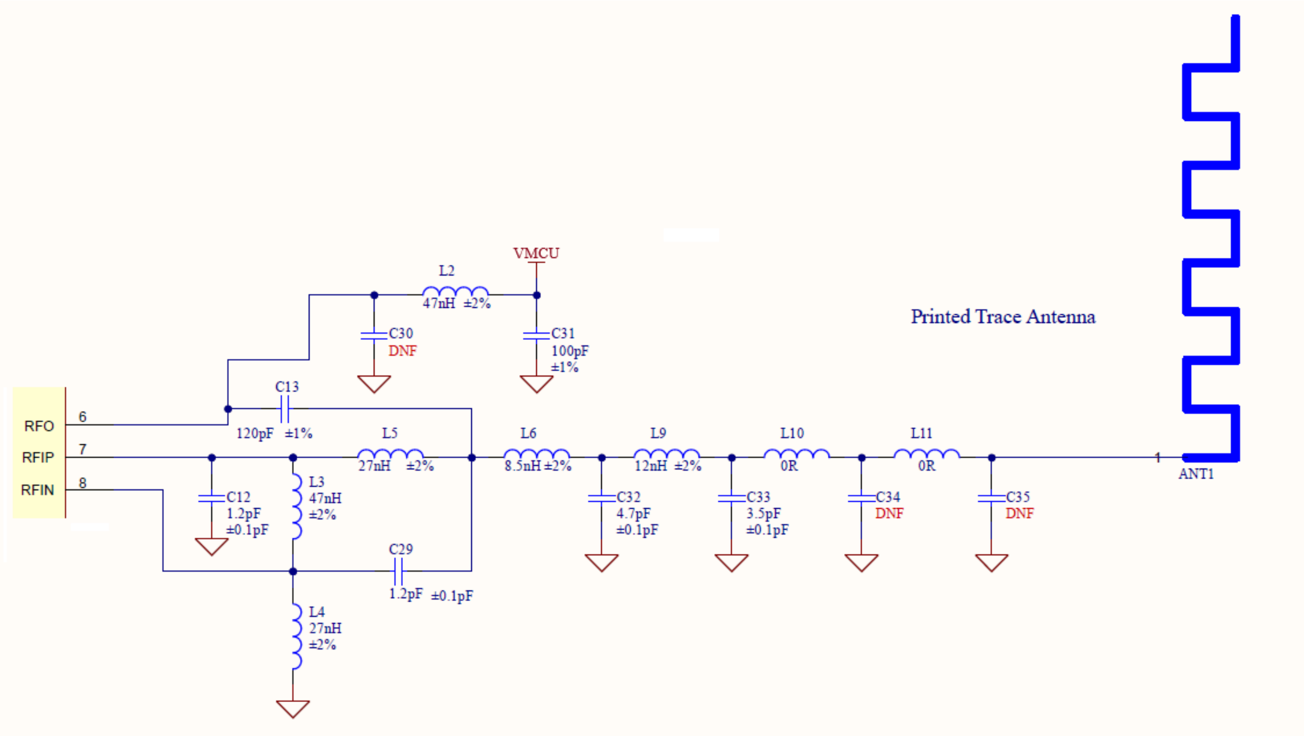

Figure 7-2 Reference RF Matching Network for +20 dBm Output Power

Table 7-2 Component Value of the +20 dBm RF Matching Network

Label	Component Value
L2, L3	47 nH ±2%
L4, L5	27 nH ±2%
L6	8.5 nH ±2%
L9	12 nH ±2%
C12, C29	1.2 pF ±0.1pF
C13	120 pF ±1%
C31	100 pF ±1%
C32	4.7 pF ±0.1pF
C33	3.5 pF ±0.1pF
L10, L11	0 ohm resistor
C30, C34, C35	DNF

These component values should be suitable for most applications assuming layout recommendations are followed, but it should be noted that the antenna matching components C34, L11 and C35 will vary depending on the feed point impedance of the antenna and will most likely need to be changed.

Power Amplifier

The single power amplifier can support the maximum output power of +20 dBm or +14 dBm depending on the voltage connected to its power pin, VDD_PA. This is because the PA output power is proportional to the square of the supplying voltage and when the voltage of VDD_PA is halved, the output power will be reduced by 6 dB. Users shall decide which maximum output power will be supported and route VDD_PA to the proper voltage source on the PCB level. Table 8 lists VDD_PA voltages required for the +20 and +14 dBm maximum output power respectively.

Table 8 VDD_PA Voltages and Tx Current for +14 and +20 dBm Maximum Output Power

Maximum Output Power	VDD_PA Voltage	Tx Current
+20 dBm	3.3 V, from VBAT	83 mA
+14 dBm	1.6 V, from DCDC	25 mA

The Fractional-N RF PLL

The RF PLL is used to generate the desired LO frequency in receiving and the RF channel frequency in transmitting. It utilizes the delta-sigma fractional-N architecture that can provide finer frequency resolution, reduced phase noise and spurs, faster lock time, lower jitter and power efficiency.

Receiver Architecture

The CZ20 employs a low-IF receiver architecture, which enhances sensitivity and selectivity for sub-GHz communication. The receiver front-end, including a Low-Noise Amplifier (LNA), a quadrature down-conversion mixer, is designed for low noise and high linearity, ensuring reliable performance in demanding RF environments. The Automatic Gain Control (AGC) module dynamically adjusts the receiver gain to prevent signal saturation, improving dynamic range and robustness against strong interferers. This ensures reliable reception in varying signal conditions, such as urban environments with high interference levels.

Additionally, the integrated Received Signal Strength Indicator (RSSI) provides real-time measurement of the received signal power, enabling applications such as adaptive power control, network optimization, and Listen Before Talk (LBT).

Transmitter Architecture

The CZ20 features a direct-conversion transmitter architecture. The modulator supports (G)FSK with configurable Gaussian filters for spectral shaping, reducing adjacent channel interference. Additionally, it supports DSSS O-QPSK with a Raised Cosine shaping filter, enhancing spectral efficiency and improving resilience against multipath fading.

The transmitter is designed for high efficiency with programmable output power, allowing optimization for long-range communication while maintaining regulatory compliance. Advanced power control mechanisms enable dynamic output adjustments, balancing power consumption and link budget requirements. The Listen Before Talk (LBT) algorithm is also supported to prevent collisions on the air.

Low Power Modes

Many IoT devices are battery powered and some of them require very long battery life. This makes the current consumption very critical. CZ20 has several low-power modes that will provide different degrees of power saving. Those low-power modes are WFI/WFE, Sleep, Deep Sleep and Deep Power-down.

Major characteristics of those low power states are summarized in Table 9. Because states of CPU are lost in Deep Sleep and Deep Power-down modes, CPU will be reboot when waking up from these two modes.

Table 9 Summary of Low-power Modes

Power Modes	Active LDOs	Active Clocks	CPU State	Memory	Wakeup
Normal	MV DCDC/(LDO)* LV LDO Retention LDO	RCO32K XO32M (Baseband PLL)	Active WFI/WFE	On	Interrupts
Sleep	Retention LDO	RCO32K	WFI/WFE	Retention	Interrupts
Deep Sleep	Retention LDO	Off/(RCO32K)	Off	Off/(Retention)	GPIO (RTC timer)
Deep Power-down	None	None	Off	Off	GPIO

**Items inside ( ) are optional.*

Power Domains of Peripherals

In order to further reduce the leakage current in low-power modes, peripherals are partitioned into 4 power domains according to their functionalities in Sleep and Deep Sleep modes. Table 10 shows the default behaviors of each peripheral power domain in each low-power mode.

Table 10 Power Domains of Peripherals

Power Domain	Peripherals	Sleep	Deep Sleep	Deep Power-down
Always on	RTC Timer GPIO Control Watchdog Timer AUX Comparator BOD Comparator	On	On	Off
Peripherals 1	Cortex-M33 Flash Control UART 0 I2C Slave Slow-clock Timer 0/1 Security Control	On	Off	Off
Peripherals 2	PWM DMA 0/1 UART 2 QSPI 0/1 Crypto Engine I2C Master 0 I2C Master 1 AUX ADC IRM PUFrt	Off	Off	Off
Peripherals 3	Cache Control UART 1 Timer 0/1/2 FPU of Cortex-M33 DBG of Cortex-M33	Off	Off	Off

Be aware of peripherals in Peripherals 2 Power domain. Because those peripherals are powered off in Sleep mode by default, their internal states are reset to the default values after waking up from Sleep mode. It is suggested to run initialization procedures of the peripheral every time it is used.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
PMU supply voltage	V_{BATMAX}	At pin VBAT	-0.3	3.9	V
IO supply voltage	V_{IOMAX}	At pin VDD_IO	-0.3	3.9	V
PA supply voltage	V_{PAMAX}	At pin VDD_PA	-0.3	3.9	V
Analog/RF supply voltage	V_{ANAMAX}	At pin VDD_ANA/VDD_PLL	-0.3	1.26	V
Digital supply voltage	V_{DIGMAX}	At pin VDD_DIG	-0.3	1.26	V
DC voltage for GPIOs	$V_{DCIOMAX}$		-0.3	V_{IO}+0.3	V
Storage temperature	T_{STG}		-50	150	˚C
Junction temperature	T_J			125	˚C
Moisture sensitivity level	MSL			3	

ESD Rating

Parameter	Symbol	Condition		Value	Unit
Human body model	HBM	JEDEC JS-001		±2000	V
Charged device model	CDM	JEDEC JS-002		±300	V

Thermal Characteristics

Parameter	Symbol	Condition		Value	Unit
Thermal resistance, junction to ambient	Θ_{JA}			47	˚C/W
Thermal resistance, junction to case	Θ_{JC}			4.5	˚C/W

General Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating ambient temperature	T_A		-40	25	85	˚C
PMU supply voltage	V_{BAT}		1.8	3.3	3.6	V
IO supply voltage	V_{IO}		1.8	3.3	3.6	V
PA supply voltage	V_{PA}	+20 dBm		3.3		V
		+14 dBm		1.6		V
Analog/RF supply voltage	V_{ANA}	Include VDD_ANA and VDD_PLL pins.		1.1		V
Digital supply voltage	V_{DIG}			1.1		V

Boot Time

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Boot time from Power-off	$T_{BOOT-OFF}$	From power-off to CPU run		13.5		ms
Boot time from Deep-power down	$T_{BOOT-DPD}$	From deep-power down to CPU run		13.5		ms
Boot time from Deep-sleep	$T_{BOOT-DS}$	From deep-sleep to CPU run		4.0		ms

Wakeup and Sleep Time

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Wakeup from Deep Sleep*	$T_{WAKE-DS}$	Code execution from Boot ROM		2.45		ms
		Code execution from Flash		2.75		ms
Wakeup from Sleep**	$T_{WAKE-SP}$	Code execution from Flash. Divided-by-2 is enabled for rco32k.		1.94		ms
		Code execution from Flash. Divided-by-2 is disabled for rco32k.		2.75		ms
Entry time to Deep Sleep	T_{GO-DS}			240		µs
Entry time to Sleep	T_{GO-SP}	Divided-by-2 is enabled for rco32k.		197		µs
		Divided-by-2 is enabled for rco32k.		103		µs

(*)Wakeup sources from Deep Sleep can be either GPIO or RTC.
(**)Wakeup sources from Sleep can be any available interrupt.

Clock Specifications

32 MHz Crystal Oscillator

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency	F_{XO32M}			32		MHz
Equivalent series resistance	ESR				60	Ω
Load capacitance	C_L			8		pF

32 kHz RC Oscillator

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency	F_{RCO32K}			32		kHz
Calibrated frequency variation				±500		ppm
Start-up time	T_{START}			500		µs

Current Consumption

Unless otherwise indicated, typical conditions are: V_{BAT} = 3.3 V. T_A = 25 °C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current consumption of MCU per MHz	I_{MCU}	All peripherals are disabled and DCDC is used.		54.9		µA/MHz
Current consumption in Sleep 1 mode	I_{SLP1}	SoC system is in Sleep mode. Communication sub-system is in Sleep mode and wireless links are maintained. Wake up by GPIO or Timer. Slow clock is 16 kHz.		4.0		µA
		SoC system is in Sleep mode. Communication sub-system is in Sleep mode and wireless links are maintained. Wake up by GPIO or Timer. Slow clock is 32 kHz.		4.2		µA
Current consumption in Sleep 2 mode	I_{SLP2}	SoC system is in Sleep mode. Communication sub-system is in Deep Sleep mode and wireless links are lost. Wake up by GPIO or Timer. Slow clock is 16 kHz.		1.9		µA
		SoC system is in Sleep mode. Communication sub-system is in Deep Sleep mode and wireless links are lost. Wake up by GPIO or Timer. Slow clock is 32 kHz.		2.0		µA
Current consumption in Deep Sleep mode	I_{DSLP}	Wake up by GPIO only without retention memory. RC oscillator is off.		1.2		µA
		Wake up by GPIO only with 16 KB retention memory. RC oscillator is off.		1.3		µA
Current consumption in Deep Power-down mode	I_{DPD}	Wake up by GPIO only.		0.5		µA

Flash Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Flash supply voltage	VDD_{FLASH}		1.65		3.6	V
Flash data retention	RET_{FLASH}			20		years
Flash erase/program cycles	EP_{FLASH}		100,000			cycles
Flash program time	T_{PRG}	one byte		65	240	µ
		one page (256 bytes)		1	8	ms
Flash erase time	T_{ERASE}	4 KB		100	800	ms
		32 KB		0.3	3	s
		64 KB		0.5	6	s
		Whole chip (1MB)		5	30	s
Flash program current	I_{PRG}			15	30	mA
Flash program time	I_{ERASE}			15	30	mA

Sub-G RF Transceiver Characteristics

Unless otherwise indicated, typical conditions are: V_{BAT} = 3.3 V. T_A = 25 °C. V_{ANA} = 1.1 V with DC/DC enabled.

Transmit Characteristics @ 14 dBm Output Power at 908/912/916/920 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RF output power	P_{OUT}	V_{PA} = 1.6 V	-20		+14	dBm
Operating frequency	F_{OPT}	R1: FSK, 9.6 kbps and R2: FSK, 40 kbps		908		MHz
		R3: GFSK, 100 kbps		916		MHz
		LR: DSSS O-QPSK, 100 kbps		912		MHz
		LR: DSSS O-QPSK, 100 kbps		920		MHz
Frequency deviation	F_{DEV}	R1: FSK, 9.6 kbps and R2: FSK, 40 kbps	32	40	48	kHz
		R3: GFSK, 100 kbps	46.4	58	69.6	kHz
Offset EVM	EVM	LR: DSSS O-QPSK, 100 kbps	2	2.5	3	%

Transmit Characteristics @ 20 dBm Output Power at 908/912/916/920 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RF output power	P_{OUT}	V_{PA} = 3.3 V	-10		+20	dBm
Operating frequency	F_{OPT}	R1: FSK, 9.6 kbps and R2: FSK, 40 kbps		908		MHz
		R3: GFSK, 100 kbps		916		MHz
		LR: DSSS O-QPSK, 100 kbps		912		MHz
		LR: DSSS O-QPSK, 100 kbps		920		MHz
Frequency deviation	F_{DEV}	R1: FSK, 9.6 kbps and R2: FSK, 40 kbps	32	40	48	kHz
		R3: GFSK, 100 kbps	46.4	58	69.6	kHz
Offset EVM	EVM	LR: DSSS O-QPSK, 100 kbps	2	2.5	3	%

Receive Characteristics at 908/912/916/920 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Sensitivity	SENS	R1: FSK, 9.6 kbps		-112		dBm
		R2: FSK, 40 kbps		-110		dBm
		R3: GFSK, 100 kbps		-107		dBm
		LR: DSSS O-QPSK, 100 kbps		-108		dBm
Adjacent interference rejection, ±1 MHz	$C/I_{ADJ(\pm 1M)}$	R1: FSK, 9.6 kbps		-48		dB
		R2: FSK, 40 kbps		-45		dB
		R3: GFSK, 100 kbps		-42		dB
Adjacent interference rejection, ±2 MHz	$C/I_{ADJ(\pm 2M)}$	R1: FSK, 9.6 kbps		-58		dB
		R2: FSK, 40 kbps		-55		dB
		R3: GFSK, 100 kbps		-52		dB
		LR: DSSS O-QPSK, 100 kbps		-49		
Out-of-band blocking, ±5 MHz	OOB_{5M}	R1: FSK, 9.6 kbps		-65		dB
		R2: FSK, 40 kbps		-62		dB

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		R3: GFSK, 100 kbps		-59		dB
		LR: DSSS O-QPSK, 100 kbps		-54		dB
Out-of-band blocking, ±10 MHz	OOB_{10M}	R1: FSK, 9.6 kbps		-67		dB
		R2: FSK, 40 kbps		-64		dB
		R3: GFSK, 100 kbps		-61		dB
		LR: DSSS O-QPSK, 100 kbps		-59		dB
RSSI			-100		0	
Note: All data is under the condition of full calibrations.						

Application Circuits

Application Circuit for +14 dBm Transmit Power

VMCU = 3.3VDC supply voltage

VDCDC = 1.6VDC from DCDC of CZ20

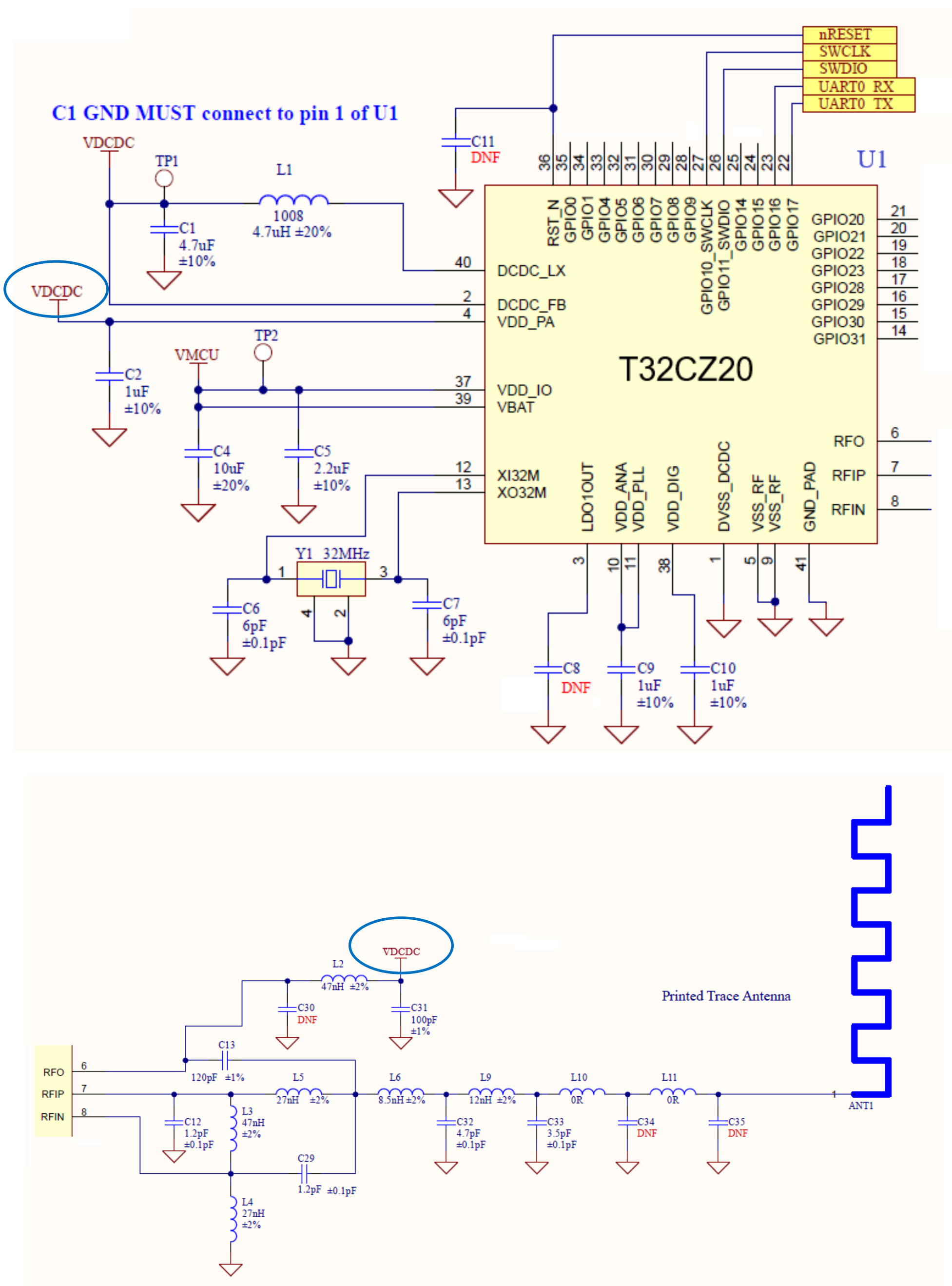

Figure 8 Application Circuit for +14 dBm Transmit Power

Application Circuit for +20 dBm Transmit Power

VMCU = 3.3VDC supply voltage

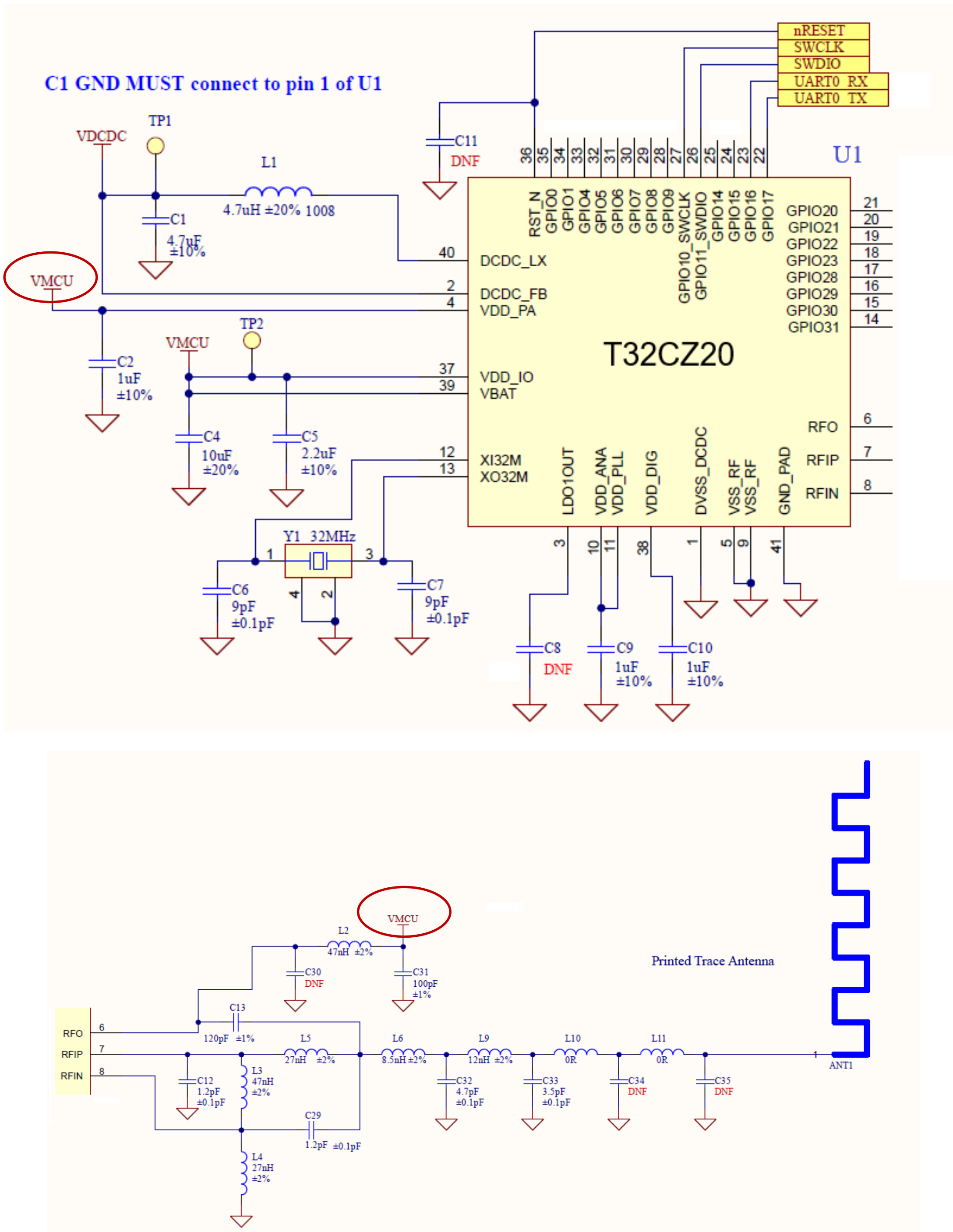

Figure 9 Application Circuit for +20 dBm Transmit Power

Package Specifications

Package Dimensions

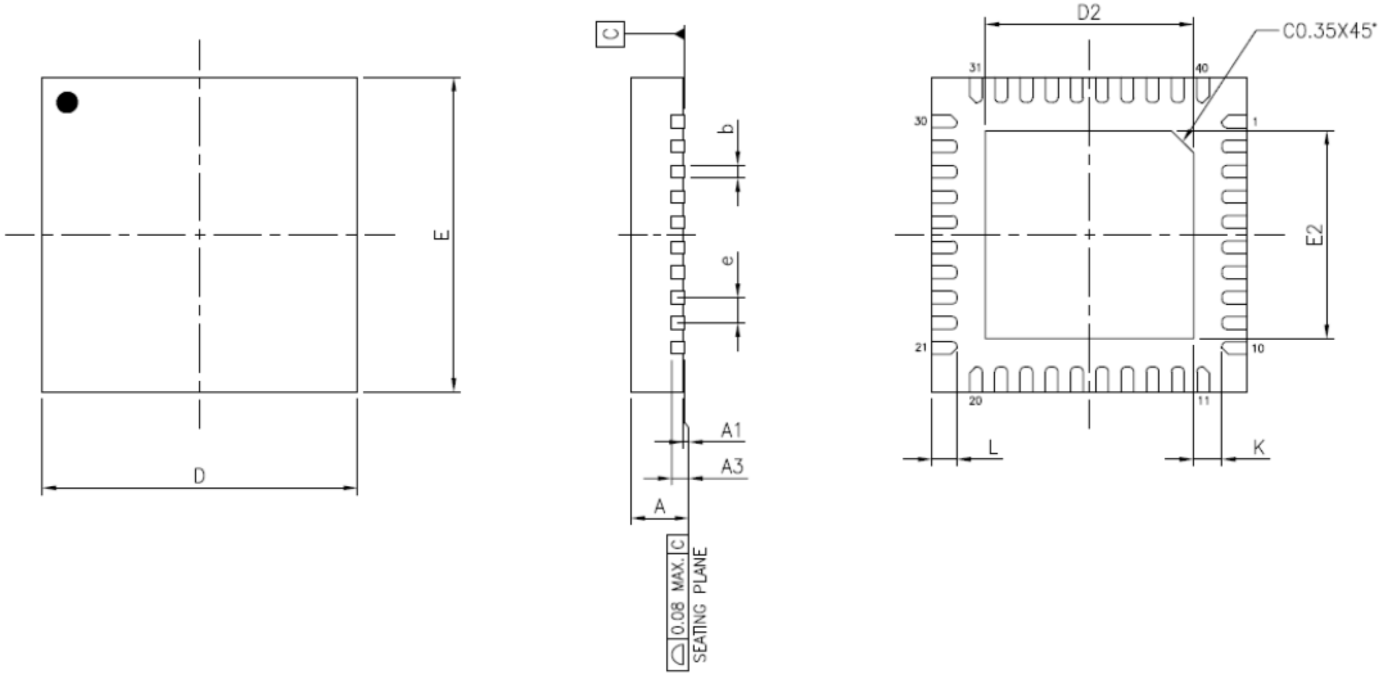

Figure 10 QFN Package Drawing

	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN 5X5 40L		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	-	-
D2	3.25	3.30	3.35
E2	3.25	3.30	3.35

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Package Marking

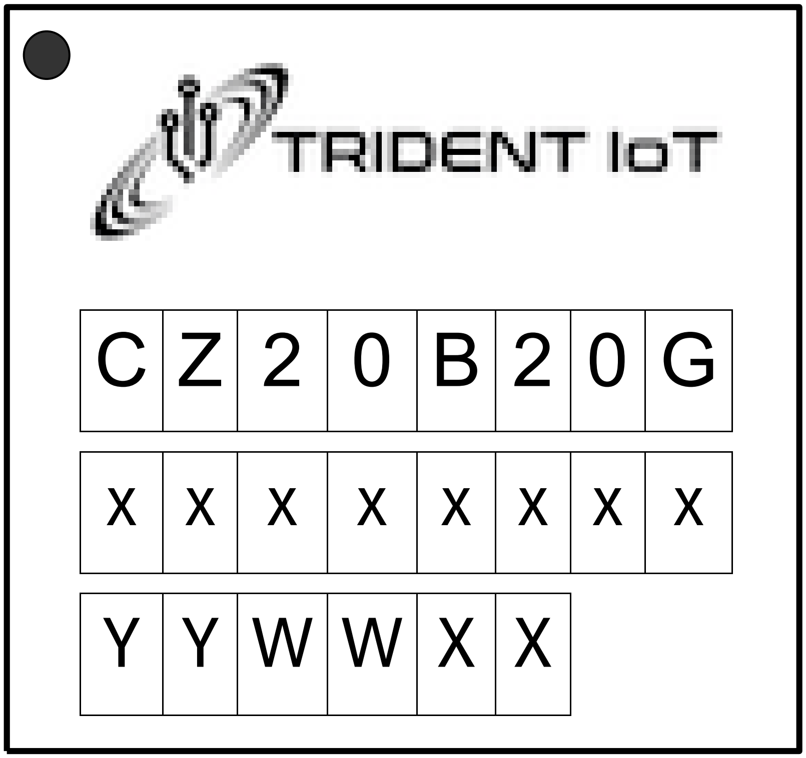

Figure 11 T32CZ20 Package Marking

Mark Method	Laser	
Font Size	Logo：4.1mm x 1.7mm Device Number：0.45mm x 0.3mm Mfg Code & Date Code：0.45mm x 0.3mm	
Line 1 Marking	Circle = 0.25mm Diameter (Top-left justified)	Pin 1 identifier
Line 2 Marking	Device Number	CZ20B20G
Line 3 Marking	XXXXXXXX = Mfg. Code	Manufacturing code varies by batch.
Line 4 Marking	YYWWXX YY = Year; WW = Work Week XX = Control Code	Year & work week of the mold date. Trident IoT internal control code

Revision History

Revision	Date	Description
0.7	March 31, 2025	• Beta Release

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