Hardware Guide

T32CZ20
Z-Wave Sub-GHz RF SoC

Description

The T32CZ20 is an ultra-low power, high performance Sub-GHz wireless SoC supporting Z-Wave to facilitate sensor network, building automation, smart locks and smart home applications. This document is to guide design engineers seeking to integrate the "CZ20" in hardware designs.

Part Number Information

Table 1 T32CZ20 Part Number Information

Part Number	Type	Package	Shipping
T32CZ20B20GQ40-AR	SoC	QFN5x5 - 40	Reel (R)
T32CZ20B20GQ40-AT	SoC	QFN5x5 - 40	Tray (T)

Development Kits

Table 2 Dev Kit Information

Part Number	Part Name	Description
DKNCZ20B20-02	Z-Wave Eval Kit CZ20	Evaluation board with PCB trace antenna, limited I/O, and integrated SEGGER J-Link onboard programmer and debugger. USB or CR2450 coin cell powered.
DKRCZ20B20-25	Z-Wave Radio Board CZ20	Development board with selectable antenna (PCB trace / SMA), selectable Tx Power (+14 / +20 dBm). Use with HOST Board.
DKR-HOST-00-A	Main Development Board	Development board with integrated SEGGER J-Link onboard programmer and debugger, full I/O breakout. Compatible Trident Radio Boards plug into the HOST Board. USB or externally powered.

[Insert sub-sections with pictures and features summary?]

Programming and Debugging Interface

The Trident Development Kits features an onboard SEGGER J-Link (J-Link OB) debugger microcontroller, which is not user-programmable and connects via the USB Type-C port. The J-Link OB enables code downloading, debugging functionalities, and provides a virtual COM port for general-purpose serial data transfer. The diagram below illustrates the connection between the target T32CZ20 device and the J-Link OB.

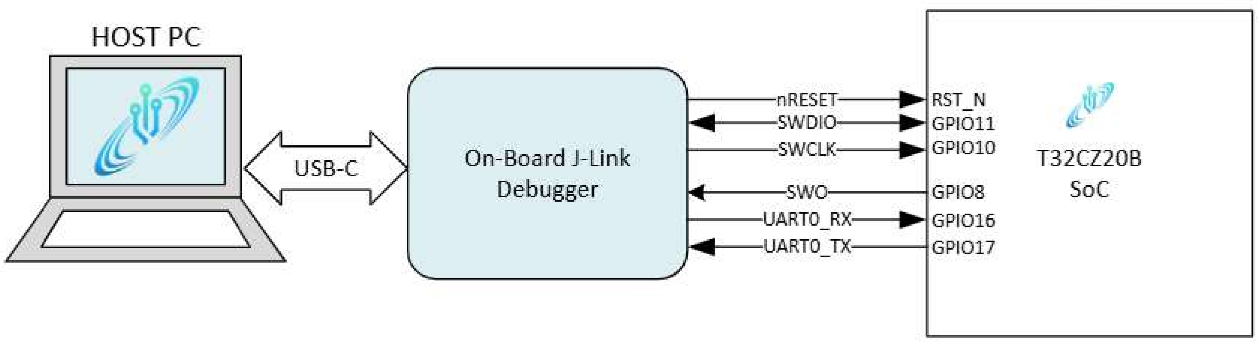
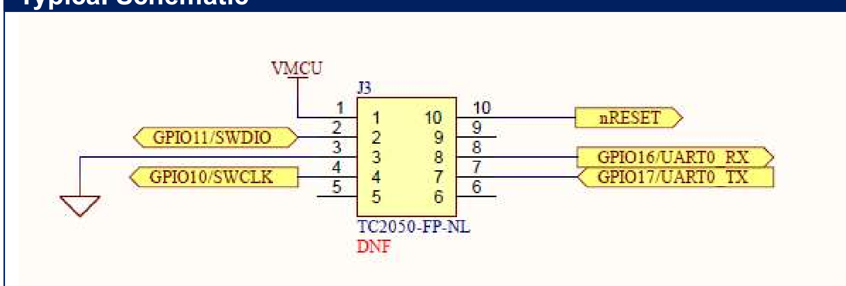
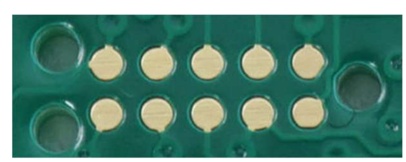


Figure-1 Programming and Debugging Overview

Dev Kit Programming Headers

When the CZ20 SoC is being added to a design, a Serial Wire Debug (SWD) interface needs to be included to program and test the SoC. For Trident Dev Kits and Reference Designs, 10-pin Tag-Connect™ TC2050-NL-FP Footprint for development use.

Table 3 Typical Programming Header

<table>
<tr><th>Typical Schematic</th><th>Typical Footprint</th></tr>
<tr><td>
</td><td>TC2050-NL-FP Footprint
</td></tr>
</table>

Note: The similar 6-pin footprints on Trident hardware are for factory use only, and not for use in development.

*Table 4 Typical Programming Header Pin-out**

Pin No.	Pin Name	Description
1	VMCU	3.3V DC Supply Voltage
2	GPIO11 / **SWDIO**	Serial Wire Data
3	GND	Ground connection
4	GPIO10 / **SWCLK**	Serial Wire Clock
7	GPIO17 / **UART0_TX**	UART Data Transmitted from CM11 / Received by connected HOST
8	GPIO16 / **UART0_RX**	UART Data Received by CM11 / Transmitted by Connected HOST
10	nRESET	Pulled low to reset the CM11
6	*Reserved*	Reserved for future use as Serial Wire Output (SWO)
5, 9	NC	No connection

**The Serial Wire and UART0 lines can be re-configured to other GPIO, the associations shown here are the default.*

Dev Kit Programing Cable

Tag-Connect TC2050 10 Pin “No legs” Plug-of-Nails™ cables TC2050-IDC-NL, TC2050-IDC-NL-050-ALL, or equivalents, can be used with DKR-HOST board to program an external target board with a TC2050-NL-FP Footprint.

Serial UART

Serial Interface

The CZ20 supports up to three (3) UART interfaces, two with flow control. The default configuration allows communication on UART0.

Table 5 Default I/O Assignments for SWD and UART0

Pin No.	Pin Name	Type	Description
22	GPIO17	DIO	multi-function digital I/O, default UART0_TX
23	GPIO16	DIO	multi-function digital I/O, default UART0_RX
26	GPIO11	DIO	multi-function digital I/O, default ARM MCU ICE data (SWDIO)
27	GPIO10	DIO	multi-function digital I/O, default ARM MCU ICE clock (SWCLK)

The Trident Evaluation and Development Kits listed in Table 2 have built-in hardware support though the On-board J-Link Debugger for serial communication with UART0 at the default GPIO. See the Dev

Kit Manual for more details.

If other serial cables or adapters are used, they must support +3.3V TTL level UART signals. Example: FTDI TTL-232R-3V3

PC Serial Interface Configuration

This example assumes a default baud rate of 230400.

1. Connect Dev Kit or Sample Device via USB cable to a computer containing a serial emulator, such as TeraTerm or PuTTY.

2. Select the communication port (COM port) ID assigned by the HOST PC to the attached

3. Set serial port configurations:
    - Baud: 230400
    - Data: 8 Bit
    - No parity
    - 1 Stop bit
    - No Flow Control

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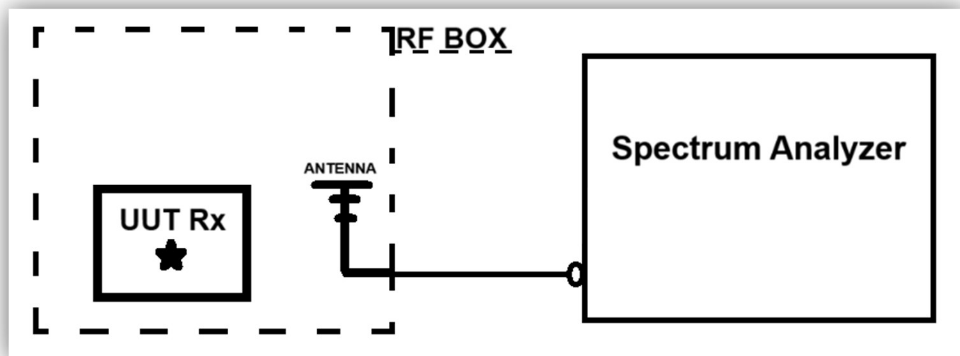
Calibration

Crystal Calibration

Devices designed with the T32CZ20 SoC will require a crystal calibration process to ensure accurate frequency control and stable operation. Trident CLI supports this process.

Calibration Setup



General Procedure:

1. Setup Spectrum Analyzer center frequency to 916MHz
2. Place UUT in RF shield box
3. Send command to UUT to start constant Transmit on 916MHz using CLI or compiled app.
4. Check transmit frequency of UUT with spectrum analyzer
5. If center frequency **is not** within ±1ppm (±916Hz) of 916MHz
    a. Try XTAL_TRIM value by sending command to UUT
    b. If the transmit frequency is LOWER THAN 916MHz, then decrease the trim value
    c. If the transmit frequency is HIGHER THAN 916MHz, then increase trim the value
    d. Repeat until acceptance criteria is met, then move to step 6
6. If center frequency **is** within ±1ppm of 916MHz
    a. Store trim value on UUT using CLI or compiled app
7. Reset UUT by power cycle

As an alternative, Trident TZM8202 modules come pre-calibrated from the factory.

Schematic

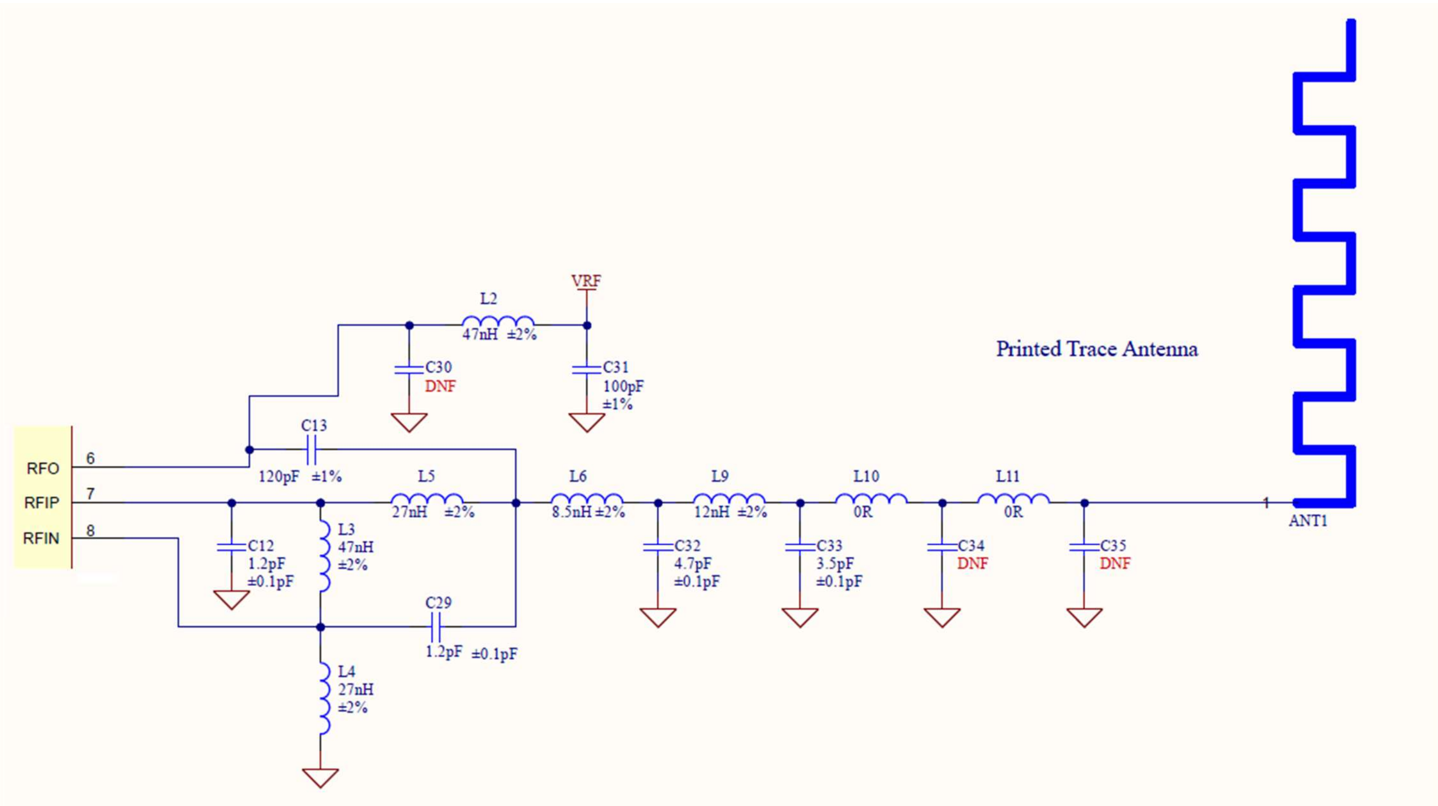
RF Interface, Harmonic Filtering and Matching

The sub-GHz RF interface on the T32CZ20B consists of a single-ended output pin (RFO) for transmitting and differential input pins (RFIP, RFIN) for receiving.

The RF matching network for the T32CZ20B will generally consist of a discrete balun section, a low-pass filter section, and an antenna impedance matching section. The balun section is used to convert a single-ended receive signal into a differential signal at the RF input pins. The low-pass filter is designed to suppress transmitter harmonics, ensuring compliance with regulatory spectral emission limits while still allowing good overall signal transmission efficiency in both directions for transmit and receive. The antenna matching section is used to match the feed point impedance of the antenna to the impedance of the filter section, which is usually chosen to be close to 50 ohms.

Typical RF Matching Network

The reference RF matching network for the T32CZ20B is shown in the application schematic below.



The balun consists of C12, L4, L3, L5 and C29.

C13 connects the RFO pin to the single ended low pass filter section at L6, and blocks the DC voltage that is supplied to the RFO pin through L2.

The low pass filter section consists of L6, L9, L10, C32 and C33.

The antenna matching Pi network consists of C34, L11 and C35.

These component values should be suitable for most applications assuming layout recommendations are followed, but it should be noted that the antenna matching components C34, L11 and C35 will vary depending on the feed point impedance of the antenna and will most likely need to be changed.

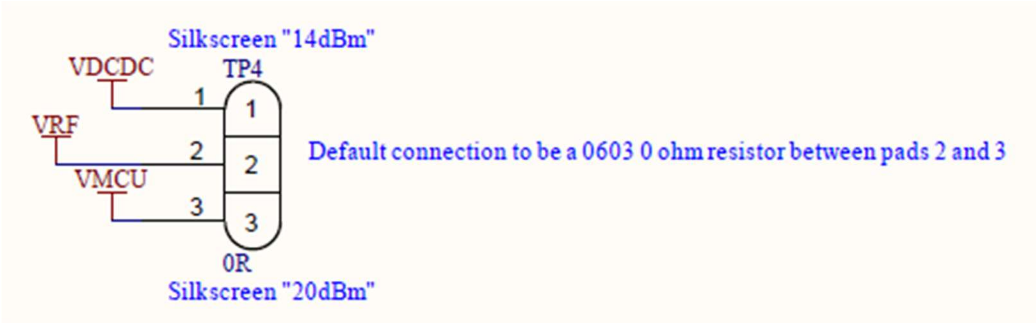
Component Values of the RF Matching Network

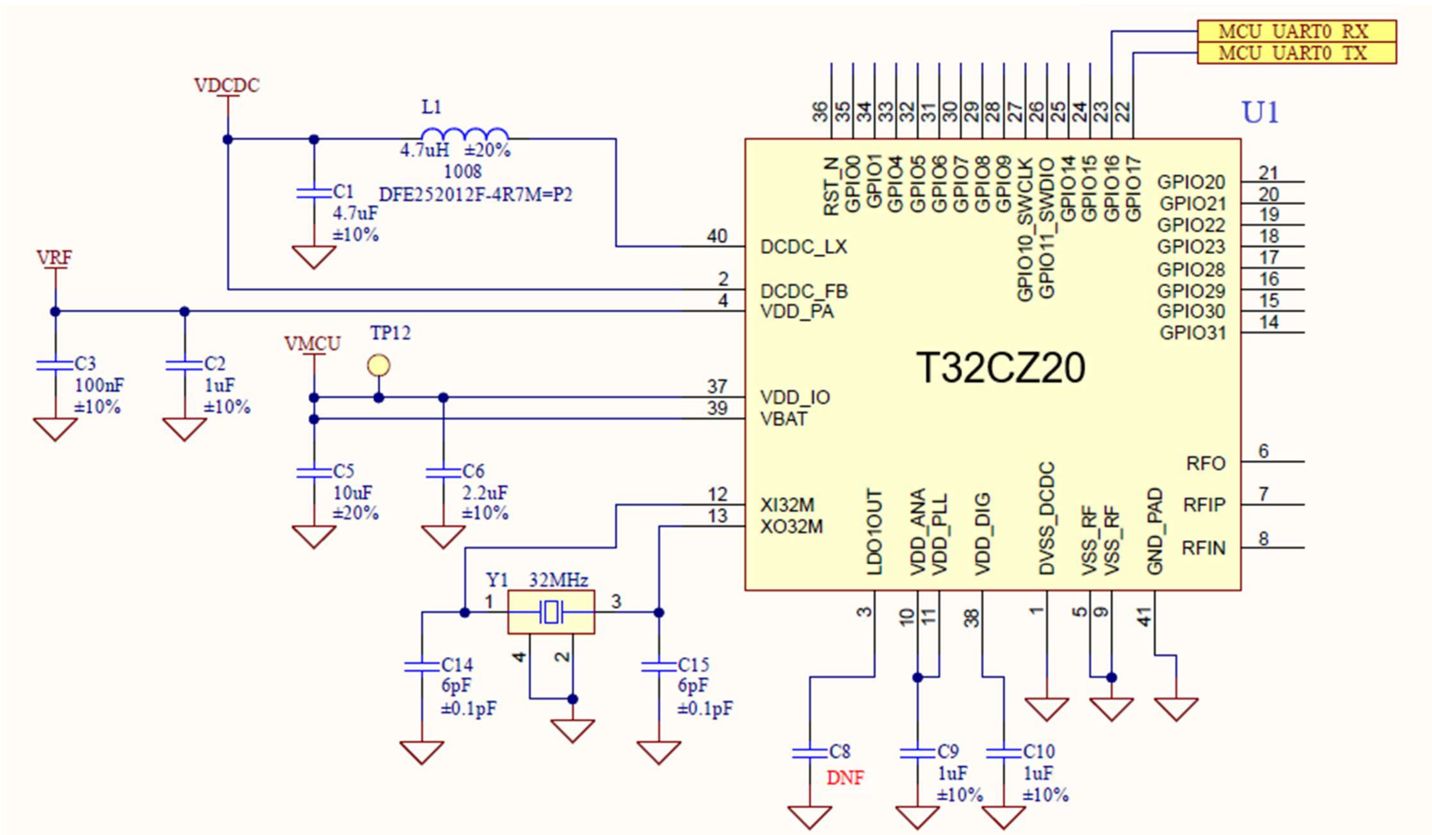
Label	Component Value
L2, L3	47 nH ±2%
L4, L5	27 nH ±2%
L6	8.5 nH ±2%
L9	12 nH ±2%
C12, C29	1.2 pF ±0.1pF
C13	120 pF ±1%
C31	100 pF ±1%
C32	4.7 pF ±0.1pF
C33	3.5 pF ±0.1pF
L10, L11	0 ohm resistor
C30, C34, C35	DNF

Power Amplifier

The RF power amplifier inside the T32CZ20B, which is connected to the RFO pin, can produce maximum output power levels of approximately +20 dBm or +14 dBm, depending on the DC voltage supplied to the VRF net which connects to L2 and to the VDD_PA pin. This is because the PA output power is proportional to the square of the supplying voltage and when the voltage of VDD_PA is halved, the output power will be reduced by approximately 6 dB. Users will need to decide which maximum output power will be supported and route VRF to the proper voltage source on the PCB.

This reference includes a solder bridge to select the desired power.





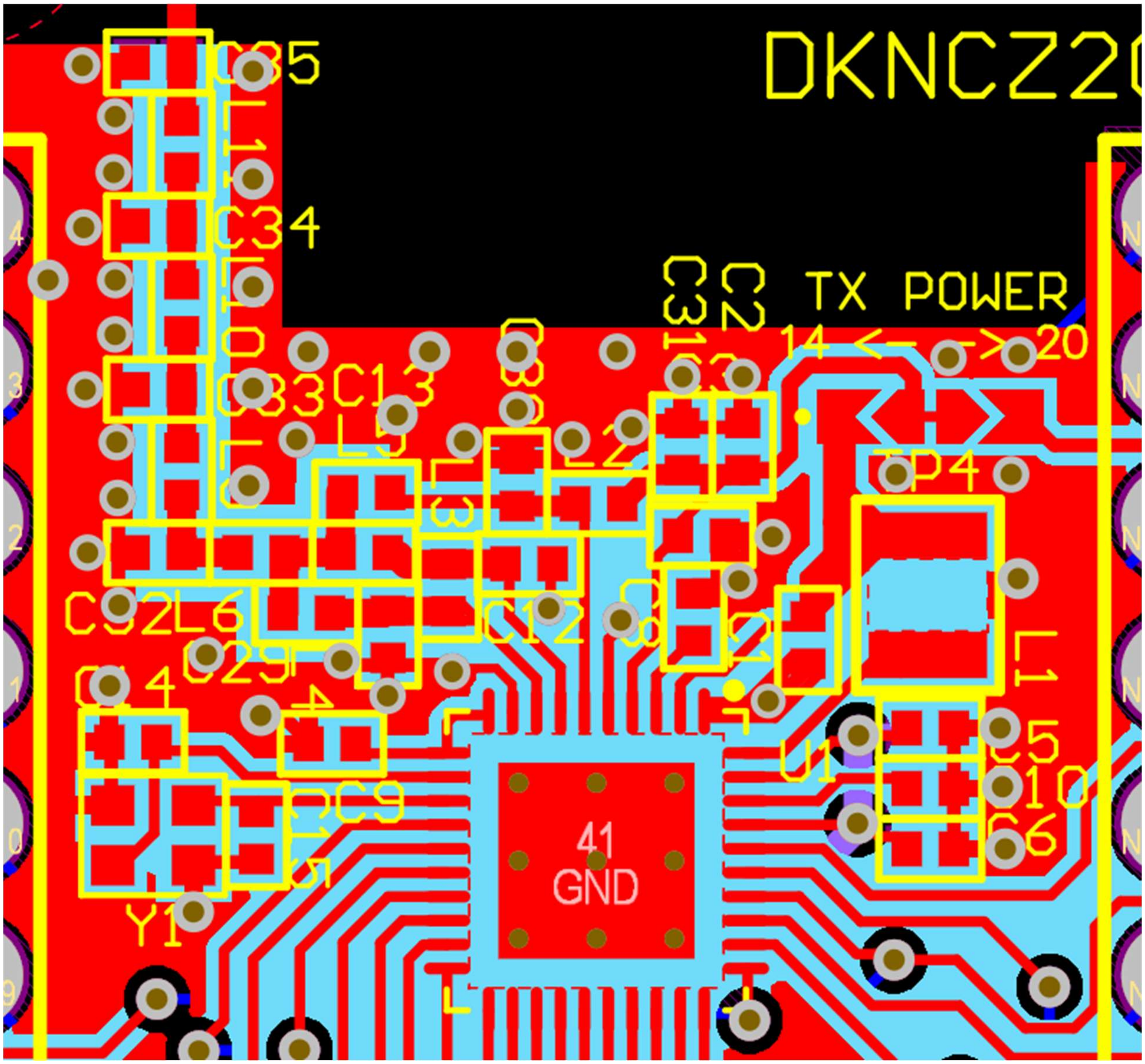
The diagrams above show options to connect VRF to 3.3VDC (VMCU) for up to +20 dBm operation, or to connect VRF to 1.6 VDC (VDCDC) for up to +14 dBm operation.

PCB Layout

Proper PCB layout and impedance control are critical for minimizing losses, optimizing RF performance and meeting regulatory requirements. Some general rules that should be followed whenever possible are:

- Keep the RF layout from the T32CZ20B to the antenna as compact as possible and keep trace length short.
- Maintain continuous solid ground plane under the RF section to minimize inductance and path length between ground connections.
- Capacitors that connect to ground in the low pass filter and matching sections (such as C32, C33, C34 and C35) should have pads on the signal path to minimize series inductance. They should not be connected to the signal path by a trace.
- If long traces must be used in the RF signal path, they should be designed for a controlled impedance that is matched at both ends to reduce reflections and losses.
- Use multiple ground vias to reduce net inductance on RF components where space permits.
- Do not connect any of the T32CZ20B ground pins on the edge of the device to the central ground pad under the T32CZ20B. This may introduce noise into the radio circuits and degrade performance.
- Connect the ground side of the capacitor C1 in the DC-DC converter directly to the DVSS_DCDC pin (pin 1) of the T32CZ20B.
- Keep DC-DC converter components C1 and L1 close to the T32CZ20B with short direct connections to minimize radiated noise.

The diagram below shows a typical PCB layout for the T32CZ20B:


C35
C34
TX POWER
14 <-- --> 20
C13
L5
L2
TP4
L1
C12
C32
L6
C29
U1
C5
C10
C6
C9
41
GND
Y1

Revision History

Revision	Date	Description
0.1		Beta Release

Related Documentation

	Document ID	Description
Data Sheet	**DS-ZW-0001-01**	Datasheet: T32CZ20 Z-Wave Sub-GHz RF SoC
Manual	**MAN-ZW-0002-01**	Manual: T32CZ20 Reference Manual

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