TRIDENT IoT

T32CM11

Zigbee / Multi-protocol 2.4-GHz RF SoC

Description

The T32CM11 is an ultra-low power, high-performance ARM® Cortex®-M3 based Zigbee 3.0 RF SoC with multi-protocol Bluetooth Low Energy 5.3, Thread/Matter, and proprietary 2.4G networking stack compatibility to facilitate home & building automation, smart lighting, smart locks, sensor network applications, etc. A comprehensive mix of analog and digital peripherals are integrated with the 2.4GHz RF transceiver which is compliant with Zigbee 3.0 and IEEE® 802.15.4 requirements. Ultra-low current consumption is achieved in the RF receive & transmit modes and power-down mode to support the latest IPv6-based IoT applications.

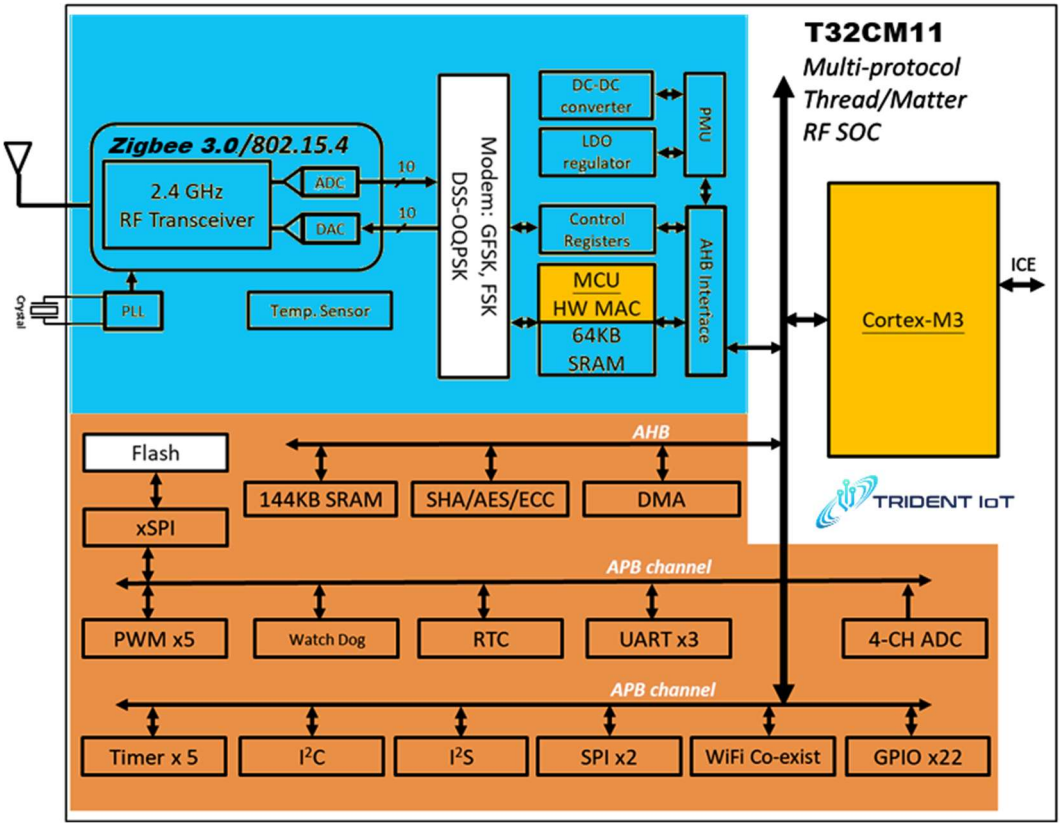


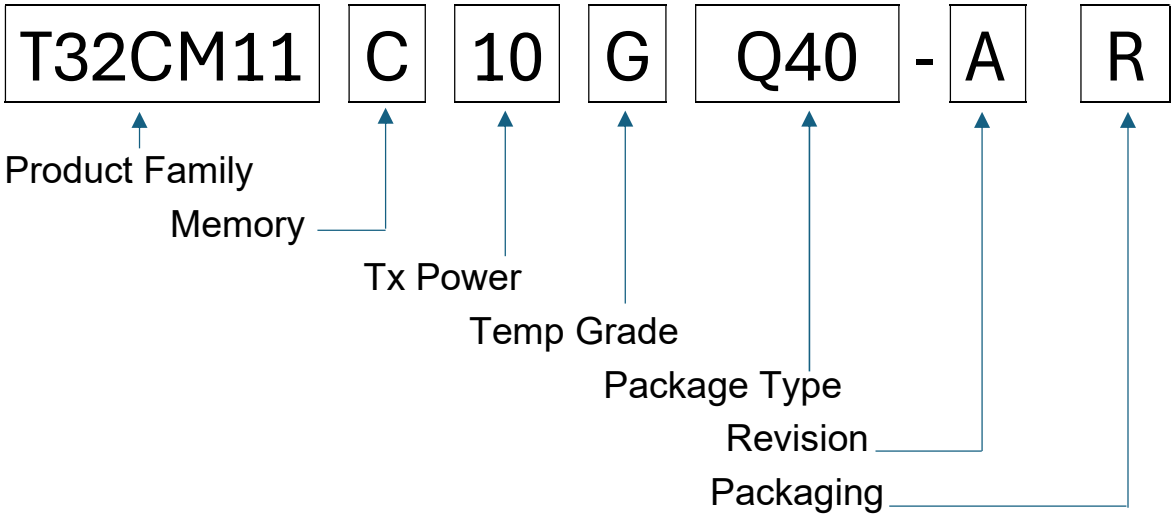
Figure 1. T32CM11 Block Diagram

Feature List

- Transmit Power
  - Zigbee/Thread: + 10dBm with <2% EVM
  - Bluetooth Low Energy: + 10dBm
- Receive Sensitivity
  - Zigbee/Thread: -100dBm
  - Bluetooth Low Energy: -104dBm@125kbps
- Supported Modulations
  - multi-rate FSK, GFSK
  - DSSS-OQPSK
- Data Rates
  - Zigbee/Thread: 250Kbps
  - Bluetooth Low Energy: 125K/500K/1M/2Mbps
- Multi-protocol support: Bluetooth® Low Energy 5.3 & IEEE 802.15.4, Zigbee 3.0
- Supports Thread/Matter applications with Bluetooth Low Energy commissioning
- RF offset cancellation loop
- Frequency hopping capability
- Programmable channel filter bandwidth
- External 32MHz high frequency crystal & internal low frequency RC Oscillator
- + 1.8 ~ + 3.6VDC Operating Voltage
  - POR (power-on reset) & UVLO (under voltage-lockout)
  - Power Management Unit for power state switching
  - Integrated DC-DC converter and LDO regulator
  - Power Saving Mode Sleep1: 5.2 μA
- Embedded ARM® Cortex-M3 CPU, internal MCU for MAC
  - ARM® CPU speed: 32M/48M/64MHz
  - SWD (2-pin Serial Wire Debug)
  - 32KB Boot ROM
  - 208KB SRAM (CPU+MCU)
  - 2048 KB Flash
- Multiple integrated peripherals
  - Integrated security: SHA/AES/ECC
  - DMA controller
  - UART interface x3 (1 with CTS/RTS, 2 without CTS/RTS)
  - I^2S interface
  - I^2C master interface
  - SPI interface x2
  - PWM x 5
  - 32-bit Timer x5
  - 32-bit Real Time Clock Timer x2
  - Temperature Sensor
  - 4CH 12-bit 350Ksps ADC
  - GPIO (w/interrupt) x22
  - WiFi Co-existence interface
  - Watchdog x1
- Package
  - Lead-Free 5x5 40-pin Quad Flat No-lead (QFN)
  - Halogen-free / RoHS 2.0 / Reach Annex 14 & 17
- Operating Temperature: -40ºC ~ +85/105ºC
- ESD: HBM 2KV / MM 200V, Latch-up: 150Ma

Ordering Information

Part Number	Package	Shipping	Minimum Order Quantity	Full Carton Quantity
T32CM11C10GQ40-AR	QFN5x5 – 40L	Reel (R)	2,500 pcs	12,500 pcs
T32CM11C10AQ40-AT	QFN5x5 – 40L	Reel (R)	2,500 pcs	12,500 pcs



Field	Values
Product Family	T32CM11: Wireless 2.4GHz Zigbee RF SoC
Memory	C = 2048kB
Tx Power	10 = 10dBm
Temp Grade	G = General (-40°C to +85°C) A = Automotive (-40°C to +105°C)
Package Type	Q40 = QFN 40
Revision	A = Revision A
Packaging	R = Tape & Reel T = Tray

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1. Overview

The T32CM11 (“CM11”) is an ultra-low power, high-performance ARM® Cortex®-M3 based Zigbee 3.0 RF SoC with multiprotocol Bluetooth Low Energy 5.3, Thread/Matter and proprietary 2.4G networking stack compatibility to facilitate home & building automation, smart lighting, smart locks, sensor network applications, etc. A comprehensive mix of analog and digital peripherals are integrated with the 2.4GHz RF transceiver which is compliant with Zigbee 3.0 and IEEE® 802.15.4 requirements. Ultra-low current consumption is achieved in the RF receive & transmit modes and power- down modes to support the latest IPv6-based IoT applications.

The T32CM11 consists of a main system and a wireless subsystem with 208KB total SRAM:

- The main system contains a 32MHz/48MHz/64MHz 32-bit ARM Cortex-M3, 144KB SRAM and 2048KB Flash for application requirements
- The 2.4GHz wireless communication subsystem has a baseband MCU processor and a HW MAC accelerator utilizing 64KB SRAM for dynamic switching between standard protocols to support multiple unique simultaneous links.

2. Pin Assignments

QFN5x5-40L Package

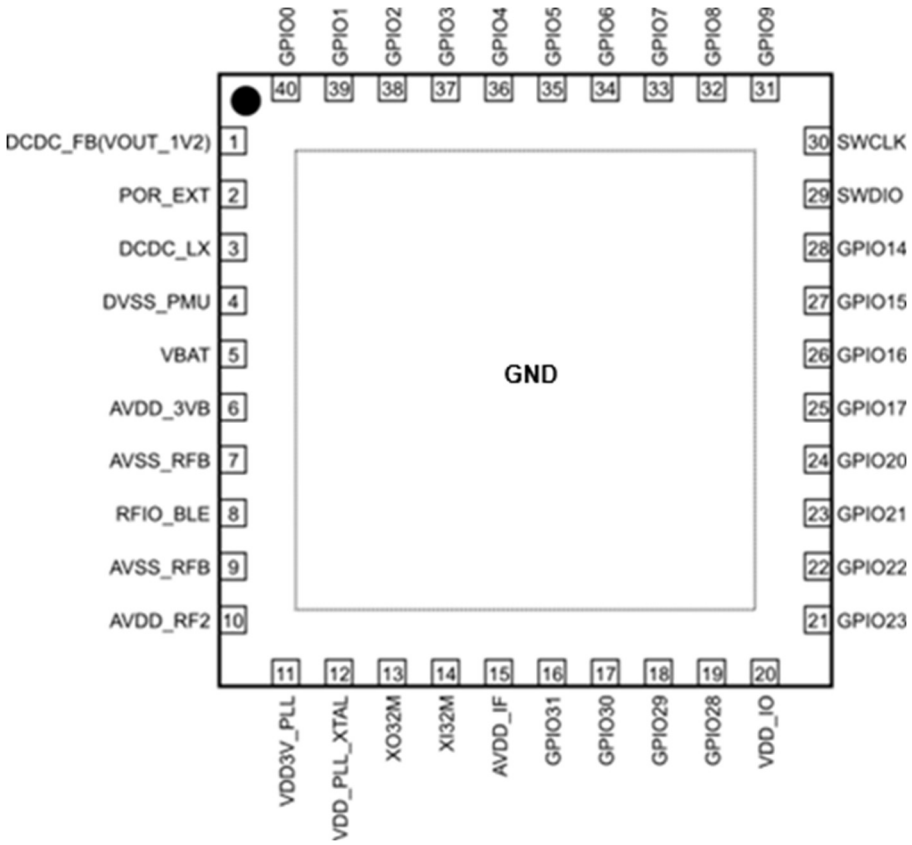


Table 1 Pin Assignments for CM11 QFN-40 package

No.	Pin Name	Type	Description
1	DCDC_FB(VOUT_1V2	power	DCDC feedback/output of internal 1.2V LDO
2	POR_EXT	DI	external Power-on Reset input
3	DCDC_LX	power	1.2VDC output of DC-DC converter
4	DVSS_PMU	ground	ground for Power Management Unit
5	VBAT	power	3.3VDC for Power Management Unit
6	AVDD_3VB	power	3.3VDC for 2.4GHz Power Amplifier
7	AVSS_RFB	ground	ground for 2.4GHz RF block
8	RFIO_BLE	RF	2.4GHz RF input/output
9	AVSS_RFB	ground	ground for 2.4GHz RF block
10	AVDD_RF2	power	1.2VDC for LNA and RF blocks (2.4GHz)
11	VDD3V_PLL	power	3.3VDC for PLL

No.	Pin Name	Type	Description
12	VDD_PLL_XTAL	power	1.2VDC for PLL and crystal oscillator driver
13	XO32M	analog	32MHz crystal oscillator driver
14	XI32M	analog	32MHz crystal oscillator driver
15	AVDD_IF	power	1.2VDC for IF
16	GPIO31	DIO	multi-function digital I/O
17	GPIO30	DIO	multi-function digital I/O
18	GPIO29	DIO	multi-function digital I/O
19	GPIO28	DIO	multi-function digital I/O
20	VDD_IO	power	3.3VDC power for GPIO
21	GPIO23	DIO	multi-function digital I/O
22	GPIO22	DIO	multi-function digital I/O
23	GPIO21	DIO	multi-function digital I/O
24	GPIO20	DIO	multi-function digital I/O
25	GPIO17	DIO	multi-function digital I/O (UART 0 TX Default)
26	GPIO16	DIO	multi-function digital I/O (UART 0 RX Default)
27	GPIO15	DIO	multi-function digital I/O
28	GPIO14	DIO	multi-function digital I/O
29	SWDIO	DIO	ARM MCU ICE data
30	SWCLK	DIO	ARM MCU ICE clock
31	GPIO9	DIO	multi-function digital I/O
32	GPIO8	DIO	multi-function digital I/O
33	GPIO7	DIO	multi-function digital I/O
34	GPIO6	DIO	multi-function digital I/O
35	GPIO5	DIO	multi-function digital I/O
36	GPIO4	DIO	multi-function digital I/O
37	GPIO3	DIO	multi-function digital I/O
38	GPIO2	DIO	multi-function digital I/O
39	GPIO1	DIO	multi-function digital I/O
40	GPIO0	DIO	multi-function digital I/O

3. Physical Ratings

Table 2 Physical Ratings

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Storage temperature	T_{STG}	- 65	~	+ 150	ºC	
Operating ambient temperature “G” Temperature Rating “A” Temperature Rating	T_A	- 40	25	+ 85 + 105	ºC	
Maximum junction temperature	T_J	-	-	125	ºC	
Thermal Resistance (Junction to ambient)	θ_{JA}		47		ºC/W	
Thermal Resistance (Junction to case)	θ_{JC}		4.5		ºC/W	
Moisture Sensitivity Level	MSL		3			

4. Electrical Ratings

Table 3 Electrical Ratings (Rx/Tx operating mode @ 25 ºC)

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
PMU input voltage	VDD_{VBAT}	1.8	3.3	3.6	V	
Core voltage supply for Tx/Rx	VDD_{TRX}	1.08	1.2	1.35	V	
Core voltage supply for Digital	VDD_{DIG}	1.08	1.2	1.35	V	
RF input power	P_{INB}			10	dBm	2.4GHz
IO Operation Voltage	VDD_{IO}	1.8	3.3	3.6	V	

Table 4 PMU Operating Specification with VDD_{VBAT} = +3.3VDC @ 25 ºC

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
DC-DC output voltage	VDD_{1V}		1.2		V	
Max supply current load	I_{LOAD}		35		mA	
DC-DC operating current	I_{DCDC}	50	120		µA	
Small LDO output voltage	VDD_{QUIET}		0.80		V	
Small LDO operating current	I_{QUIET}		600		nA	
32KHz RC Oscillator current	I_{32K}		700		nA	

5. ESD Immunity

Table 5 ESD Immunity with VDD_{VBAT} = +3.3VDC @ 25 ºC

Characteristic	Symbol	Minimum	Unit	Condition
Machine Model	MM	± 200	V	
Human Body Model	HBM	± 2000	V	Class 2, ANSI/JEDEC JS-001
Charged Device Model	CDM	± 300	V	Class C4, ANSI/ESD STM5.3.1
Latch-up Immunity	LU	150	mA	

Note: Stresses listed in Tables 3, 4 and 5 (above) may cause permanent damage to the device. These are stress ratings only. The functional operation is not implied at these or any other conditions, as well as those indicated in the operating listings of this specification. Exposure to maximum rating conditions for extended periods may affect device performance and/or reliability.

6. 32MHz Crystal Specification

Table 6 32MHz Crystal Specifications with VDD_{VBAT} = +3.3VDC @ 25 ºC

Characteristic	Value
Nominal Frequency	32MHz
Frequency Tolerance	≦ ±20 ppm
Equivalent Series Resistance (ESR)	60 ohm maximum
Drive Level	0.1 mW maximum
Load Capacitance	9 pF typical

7. Low Frequency RC Oscillator Characteristics

Table 7 Low Frequency RC Oscillator Characteristics with VDD_{VBAT} = +3.3VDC @ 25 ºC

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Untrimmed Frequency	F_{LF}		40		KHz	
Frequency Accuracy	F_{CAL}		± 500		ppm	after trim
Start-up Time	F_{START}		300		µs	

8. RF Transceiver Characteristics

Unless otherwise indicated, typical conditions are: VDD_{VBAT} = +3.3 VDC, Temperature = 25 ºC, AVDD_RF2 = AVDD_PLL = AVDD_XTAL = AVDD_IF = 1.2 V powered from DCDC.

8.1. RF Transmitter Characteristics for GFSK

Table 8 Transmitter Characteristics for GFSK

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
RF Output Power	P_{out}	−10		+10	dBm	
Operating Frequency	$F_{OPERATING}$	2402		2480		
Frequency Drift	ΔF		< ± 50		kHz	
Frequency Drift Rate	$F_{\Delta F}$		< ± 20		kHz / 50µs	

Table 9 GFSK Transmitter Characteristics for 2.4 GHz at 1 Mbps

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Average Frequency Deviation (data pattern = 111000…)	Δf1	225	250	275	kHz	
Instantaneous Deviation (data pattern = 111000…)	Δf2	185			kHz	
Deviation Ratio	Δf2 / Δf1		80		%	
Spectrum Mask with Adjacent Channel Offset: ± 2MHz			-20		dBm	
Spectrum Mask with Adjacent Channel Offset: ≥ 3MHz			-30		dBm	

Table 10 GFSK Transmitter Characteristics for 2.4 GHz at 2 Mbps

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Average Frequency Deviation (data pattern = 111000…)	Δf1	450	500	550	kHz	
Instantaneous Deviation (data pattern = 111000…)	Δf2	370			kHz	
Deviation Ratio	Δf2 / Δf1		80		%	
Spectrum Mask with Adjacent Channel Offset: ± 4MHz			-20		dBm	
Spectrum Mask with Adjacent Channel Offset: ± 5MHz			-20		dBm	
Spectrum Mask with Adjacent Channel Offset: ± 6MHz			-30		dBm	

8.2. RF Receiver Characteristics for GFSK

Table 11 GFSK Receiver Characteristics @ 2.4GHz

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
RF Sensitivity	SENS		-93		dBm	2Mbps
			-96		dBm	1Mbps
			-99		dBm	500Kbps
			-104		dBm	125Kbps

The target signal for channel selectivity measurements = −67 dBm with modulated interference, BER = 0.1 %.

Table 12 GFSK Receiver Characteristics for 2.4GHz at 1 Mbps

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Signal to Co-Channel Selectivity	$C/I_{CO\text{-}CHANNEL}$		+6.5		dBc	
Carrier-to-Interference: -1MHz Adjacent Channel Selectivity	C/I_{-1MHz}		−5		dBc	
Carrier-to-Interference: +1MHz Adjacent Channel Selectivity	C/I_{+1MHz}		−5		dBc	
Carrier-to-Interference: -2MHz Adjacent Channel Selectivity	C/I_{-2MHz}		−25		dBc	
Carrier-to-Interference: +2MHz Adjacent Channel Selectivity	C/I_{+2MHz}		−35		dBc	
Carrier-to-Interference: -3MHz Adjacent Channel Selectivity	C/I_{-3MHz}		−35		dBc	
Carrier-to-Interference: +3MHz Adjacent Channel Selectivity	C/I_{+3MHz}		−40		dBc	
Image Channel Selectivity	C/I_{IMAGE}		−25		dBc	
Image -1MHz Adjacent Channel Selectivity	$C/I_{IMAGE1MHz}$		−35		dBc	
Intermodulation Interferer Level	IM		−35		dBc	
Out-of-band Blocking: Interferer 30MHz ≤ f ≤ 2000MHz	$OOB_{30\text{-}2000MHz}$		−15		dBm	
Out-of-band Blocking: Interferer 2003MHz ≤ f ≤ 2399MHz	$OOB_{2000\text{-}2399MHz}$		−20		dBm	
Out-of-band Blocking: Interferer 2484MHz ≤ f ≤ 2997MHz	$OOB_{2484\text{-}2997MHz}$		−20		dBm	
Out-of-band Blocking: Interferer 2997MHz ≤ f ≤ 6GHz	$OOB_{2997\text{-}6000GHz}$		−10		dBm	
Out-of-band Blocking: Interferer 6GHz ≤ f ≤ 12.75GHz	$OOB_{6\text{-}12.75GHz}$		−10		dBm	
RSSI	RSSI	-90		0	dB	

Table 13 GFSK Receiver Characteristics for 2.4GHz at 2 Mbps

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Signal to Co-Channel Selectivity	$C/I_{CO\text{-}CHANNEL}$		6.5		dBc	
Carrier-to-Interference: -2MHz Adjacent Channel Selectivity	C/I_{-2MHz}		−4		dBc	
Carrier-to-Interference: +2MHz Adjacent Channel Selectivity	C/I_{+2MHz}		−4		dBc	
Carrier-to-Interference: -4MHz Adjacent Channel Selectivity	C/I_{-3MHz}		−24		dBc	
Carrier-to-Interference: +4MHz Adjacent Channel Selectivity	C/I_{+3MHz}		−30		dBc	
Carrier-to-Interference: -6MHz Adjacent Channel Selectivity	C/I_{-6MHz}		−35		dBc	
Carrier-to-Interference: +6MHz Adjacent Channel Selectivity	C/I_{+6MHz}		−40		dBc	
Image Channel Selectivity	C/I_{IMAGE}		−24		dBc	
Image -2MHz Adjacent Channel Selectivity	$C/I_{IMAGE2MHz}$		−35		dBc	
Intermodulation Interferer Level	IM		−25		dBc	
Out-of-band Blocking: Interferer 30MHz ≤ f ≤ 2000MHz	$OOB_{30\text{-}2000MHz}$		−15		dBm	
Out-of-band Blocking: Interferer 2003MHz ≤ f ≤ 2399MHz	$OOB_{2000\text{-}2399MHz}$		−20		dBm	
Out-of-band Blocking: Interferer 2484MHz ≤ f ≤ 2997MHz	$OOB_{2484\text{-}2997MHz}$		−20		dBm	
Out-of-band Blocking: Interferer 2997MHz ≤ f ≤ 6GHz	$OOB_{2997\text{-}6000GHz}$		−10		dBm	
Out-of-band Blocking: Interferer 6GHz ≤ f ≤ 12.75GHz	$OOB_{6\text{-}12.75GHz}$		−10		dBm	
RSSI	RSSI	-90		0	dB	

8.3. RF Transmitter Characteristics for DSSS-OQPSK

Table 14 DSSS-OQPSK Transmitter Characteristics for 2.4 GHz at 250 kbps

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
RF Output Power		−10		+10	dBm	
Operating Frequency		2405		2480		
EVM at rated TX power			2%			RMS
Spectrum Mask with Adjacent Channel offset			−20		dB	

8.4. RF Receiver Characteristics for DSSS-OQPSK

The wanted signal for channel selectivity measurements = −82 dBm with OQPSK PHY interference, PER = 1 %.

Table 15 DSSS-OQPSK Receiver Characteristics for 2.4GHz at 250 kbps

Parameter	Symbol	Values			Unit	Condition
		Min	Typical	Max		
RF Sensitivity			−100		dBm	
Signal to Co-Channel Selectivity	$C/I_{CO\text{-}CHANNEL}$		1		dBc	
-5MHz Adjacent Channel Selectivity	C/I_{-5MHz}		−25		dBc	
+5MHz Adjacent Channel Selectivity	C/I_{+5MHz}		−30		dBc	
-10MHz Adjacent Channel Selectivity	C/I_{-10MHz}		−45		dBc	
+10MHz Adjacent Channel Selectivity	C/I_{+10MHz}		−45		dBc	
Image Channel Selectivity	C/I_{IMAGE}		−25		dBc	
Blocking other Channels: Interferer frequency < Desired frequency			−50		dBc	
RSSI	RSSI	-90		0	dB	

9. Power

Table 12 Power Saving Mode

Mode	Internal Function Block								
	sLDO	LF OSC	XTAL	PLL	TX PA	RX	Cortex-M3 Platform	SRAM Retention	Communication
Sleep 1	ON	ON	OFF	OFF	OFF	OFF	**sleep**	32KB	standby

Table 13 Power Consumption (entire chip) with VDD_{VBAT} = +3.3VDC @ 25 ºC

Mode	Symbol	Values			Unit	Condition
		Min	Typical	Max		
Sleep 1	I_{slp1}		5.2		µA	Low power level sleep 1; wakeup by any event
Receive @ 1Mbps	$I_{RECEIVE}$		11.0		mA	Radio receiving @DCDC
Receive @ 2Mbps	$I_{RECEIVE}$		11.0		mA	Radio receiving @DCDC
Transmit @ 0dBm	I_{TX_0}		14.0		mA	Radio transmission @DCDC
Transmit @ +4dBm	I_{TX_+4}		17.0		mA	Radio transmission @DCDC
Transmit @ +10dBm	I_{TX_+10}		25.0		mA	Radio transmission @DCDC

* Receive & transmit current does not include the Cortex-M3 MCU domain current

10. Power Saving Modes

There are several power saving modes in T32CM11 that can be used to reduce power consumption.

10.1. Wait-for-interrupt State

In this mode, only the clock to the Cortex-M3 is turned off while other clocks are kept running. Any enabled interrupt will resume the Cortex-M3 clock.

10.2. Sleep state

In sleep state, the 32MHz XTAL is powered off and only the LF OSC clock is active. All peripheral interfaces such as UART, SPI, I2C, etc. are disabled. The RTC, the slow clock timer and GPIOs can be programmed to wake up the system. The data of some registers and memories are retained so the Cortex-M3 will continue running from where it stopped.

The communication subsystem can be optionally enabled to maintain active RF links. When enabled, to minimize power consumption in this condition the communication subsystem is only active during scheduled time windows. An interrupt from the communication subsystem can also wake up the entire SoC.

10.3. Power Domains of Peripherals

To further reduce the leakage current in low-power mode, peripherals are partitioned into several power domains according to their functionalities in Sleep mode. The table below shows the default behaviors of each peripheral power domain in low-power mode.

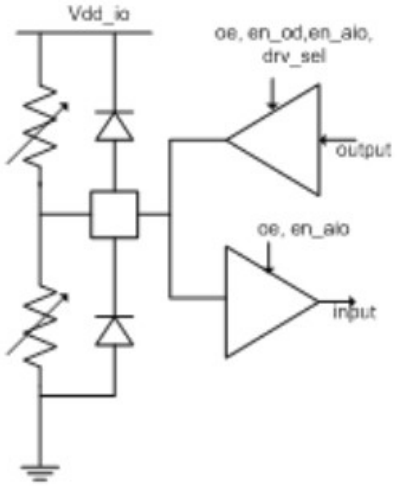
Power Domain	Peripherals	Sleep
Always On	RTC Timer GPIO Control AUX Comparator	On
Peripherals 1	Cortex-M3 Flash Control Cache Control UART 0/1 Slow-clock Timers Watchdog Timer	On
Peripherals 2	PWM DMA Timer 0/1/2 UART 2 QSPI 0/1 Crypto Engine I2C Master I2S Master AUX ADC	Off

11. Interfaces

11.1. IO

IO interfaces provide communication between the CM11 and external ICs. They support several modes such as input mode, output mode, open drain mode, Analog IO mode and they can be configured by software. The IO interfaces can also be configured by software to be SPI, UART, I2C, I2S, PWM and general purpose IO (GPIO). When used as the GPIO function, the input status also can be read by software and can be set to VDD_IO or GND by software.

The basic IO architecture is:



The IO also provides several input pull modes and output driving currents.

Input pull mode features:

- No pull (floating)
- Pull up to VDD_IO 10K/100K/1M
- Pull down to GND 10K/100K/1M

Output driving current features:

- 4mA
- 10mA
- 14mA
- 20mA

Table 14 GPIO function mux for accessing peripherals

IO	SPI0	SPI1	UART	I2C	PWM	I2S
GPIO0(OD)	SPI0_CSN1/2/3					I2S0_BCK
GPIO1(OD)	SPI0_CSN1/2/3					I2S0_WCK
GPIO2(OD)	SPI0_CSN1/2/3					I2S0_SDO
GPIO3(OD)	SPI0_CSN1/2/3					I2S0_SDI
GPIO4(OD)	SPI0_SDATA2		UART1_TX			I2S0_MCLK
GPIO5(OD)	SPI0_SDATA3		UART1_RX			I2S0_MCLK
GPIO6(OD)	SPI0_SCLK		UART2_TX			
GPIO7(OD)	SPI0_CSN0		UART2_RX			
GPIO8(OD)	SPI0_SDATA0				PWM0	
GPIO9(OD)	SPI0_SDATA1				PWM1	
GPIO14(OD)	SPI0_SDATA2	SPI1_SDATA2	UART1_RTSN		PWM2	
GPIO15(OD)	SPI0_SDATA3	SPI1_SDATA3	UART1_CTSN		PWM3	
GPIO16(OD)			UART0_RX			
GPIO17(OD)			UART0_TX			
GPIO20(OD)			UART1_RTSN	SCL	PWM0/1/2/3/4	
GPIO21(OD)			UART1_CTSN	SDA	PWM0/1/2/3/4	
GPIO22(OD)				SCL	PWM0/1/2/3/4	
GPIO23(OD)				SDA	PWM0/1/2/3/4	
GPIO28(OD)(AIO4)	SPI0_SCLK	SPI1_SCLK	UART1_TX			
GPIO29(OD)(AIO5)	SPI0_CSN0	SPI1_CSN	UART1_RX			
GPIO30(OD)(AIO6)	SPI0_SDATA0	SPI1_SDATA0	UART2_TX			
GPIO31(OD)(AIO7)	SPI0_SDATA1	SPI1_SDATA1	UART2_RX			

SDATA0 = MOSI, SDAT1 = MISO

11.2. SPI

The Serial Peripheral Interface either controls a serial data link as a master or reacts to a serial data link as a slave. Quad-bit mode (QSPI) is also supported.

The internal AHB bus controller can be configured by software to be a master or slave device. The maximum clock frequency is 16 MHz (Master mode) or 32 MHz (Slave mode). Core reading & writing is done on the AMBA AHB bus interface. The core operates in two data modes (8-bit or 32-bit). Data is serialized and then transmitted, either LSB or MSB first, using the standard 4-wire SPI bus interface or the extended Quad mode bus.
SPI interface features:

- 8- or 32-bit serial transmit & receive
- Half duplex operation
- Software programmable Master or Slave mode
- Quad-bit mode operation
- Dual-bit mode operation
- separate SCLK input for Master Mode
- 32-word Transmit FIFO
- 32-word Receive FIFO
- Interrupt control
- LSB or MSB mode
- Tristate Slave MISO signaling for multiple slaves
- DMA Interface
- Compatible with many industry-standard FLASH device

11.3. UART

The T32CM11 UART interface is compatible with 16450 and 16550. The three independent UARTs have a maximum baud rate up to 2 Mbps.

UART interface features & supported baud rates:

- 16450 & 16550 Compatible Modes
- Programmable baud rates up to 2Mbps
- FIFO and non-FIFO modes
- Transmit and Receive FIFOs
- Interrupt control
- Flow control

Supported Baud Rates (bps)
2400
4800
9600
14400
19200
28800
38400
57600
76800
115200
500000
576000
1000000
2000000

11.4. I²C

This is a standard I²C Master. A clock divider/clock select module customizes the frequency of the I²C portion of the module. Two separate FIFOs are used – one for storing up to 32 commands from the APB Interface, the other for storing up to 16 bytes of read data from the I²C Bus. The transmit engine reads commands from the command FIFO and executes these as I²C instructions. The receive engine monitors the I²C bus for slave responses and stores data in a Read Data FIFO, the contents of which are available to the processor on the APB Interface. Various conditions can cause an interrupt to be generated.

I²C interface features:

- Standard I²C (Inter-Integrated Circuit bus interface)
- Master mode only
- Transmit and Receive Engine
- Clock Divider/Clock Select
- Command FIFO and Read Data FIFO
- Interrupt Generation Logic
- Supports clock stretching
- Supports SCL arbitration

11.5. I²S

The I²S module transmits or receives audio samples with predefined protocols through GPIO. It supports two channels with I²S, LJ (Left Justified) and RJ (Right Justified) format. Two xDMA are also included in the I²S module to transfer audio samples between memory and the I²S module without CPU assistance.

The I²S interface features:

- Master mode
- Master clock generator for MCLK
- Supports Tx, Rx and Tx+Rx

- Supports I^2S, LJ and RJ format with 16/32-BCK
- Supports 16/24/32-bit sample width
- Supports 8K, 16K, 32K and 48Kbps audio sample rates
- Supports DMA

11.6. PWM

The PWM module generates Pulse Width Modulated signals and drives the assigned GPIOs. It includes a pulse generator with up and up-and-down counting mode. Five PWM modules can provide up to 5 PWM channels and each channel can have its own individual frequency control for generation of the pulse width. A read-type xDMA is also included in the PWM module to transfer frequency control between memory and PWM module without CPU assistance.

PWM features:

- Programmable clock divider
- Five PWM modules and up to five channels for PWM
- PWM pulse generator with up and up-and-down counting mode
- Programmable duty-cycle sequence defined in memory
- Duty-cycle sequence that can be repeated or loop-controlled

11.7. ADC

The ADC is an auxiliary differential successive-approximation analog-to-digital converter. The ADC module is used for measuring voltage from IO. Various sampling modes are provided, and one DMA is included for the MCU to access memory written by the ADC.

Features:

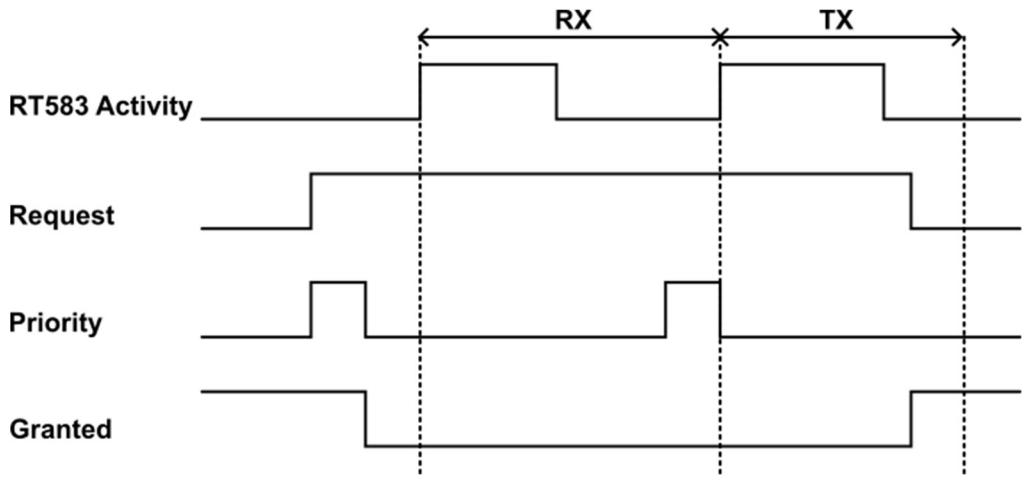
- 8/10/12-bit resolution and 14-bit resolution by oversampling
- One-shot, timer and scan mode for channel measuring
- One DMA to transfer ADC samples to memory with unsigned 16-bit format
- Monitoring ADC sample result of each channel

11.8. WiFi Coexistence

CM11 supports the common 3-wire WiFi coexistence interface. The three signals involved in this interface are:

- **Request (REQ)**: This signal is sent from CM11 to the coexistence mechanism, such as the Packet Traffic Arbitration (PTA). It indicates that the CM11 wants to transmit or receive a packet and requires access to the radio spectrum.
- **Priority (PRI)**: This signal indicates the priority of the request, typically based on whether the data being transmitted is high priority or lower priority. It helps the coexistence mechanism decide which device should be granted access to the spectrum first when multiple devices are requesting transmission.
- **Granted (GNT)**: This is the response signal from the coexistence mechanism, informing CM11 that it has been granted permission to transmit or receive its packet.

Different PTA hosts may have varying timing requirements for the three signals, and the CM11 offers flexibility to accommodate them. The timing diagram below is an example of the PTA interface.



The 3-wire interface can be configured via GPIO6, GPIO7, and GPIO8, as shown in the table below.

Pin List:

Signal	GPIO Map
Request	GPIO6
Priority	GPIO7
Granted	GPIO8

12. Radio

12.1. Antenna Interface

The 2.4 GHz antenna interface consists of a single-ended pin (RFIO_BLE). The RF matching network includes a low-pass filter designed to suppress transmitter harmonics, ensuring compliance with regulatory spectral emission limits and improving overall transmission efficiency. Proper PCB layout and impedance control are critical for minimizing losses and optimizing RF performance. For example, the RF trace should be kept as short as possible while ensuring it maintains a 50-ohm impedance to ensure signal integrity and reduce potential signal reflections.

12.2. Fractional-N RF PLL

The RF PLL is used to generate the desired LO frequency in receiving and the RF channel frequency in transmitting. It utilizes the delta-sigma fractional-N architecture that can provide finer frequency resolution, reduced phase noise and spurs, faster lock time, lower jitter and power efficiency.

12.3. Receiver Architecture

CM11 employs a low-IF receiver architecture, which enhances sensitivity and selectivity for 2.4 GHz communication. The receiver front-end, including a Low-Noise Amplifier (LNA), a quadrature down-conversion mixer, is designed for low noise and high linearity, ensuring reliable performance in demanding RF environments. The Automatic Gain Control (AGC) module dynamically adjusts the receiver gain to prevent signal saturation, improving dynamic range and robustness against strong interferers. This ensures reliable reception in varying signal conditions, such as urban environments with high interference levels.

Additionally, the integrated Received Signal Strength Indicator (RSSI) provides real-time measurement of the received signal power, enabling applications such as adaptive power control and network optimization.

12.4. Transmitter Architecture

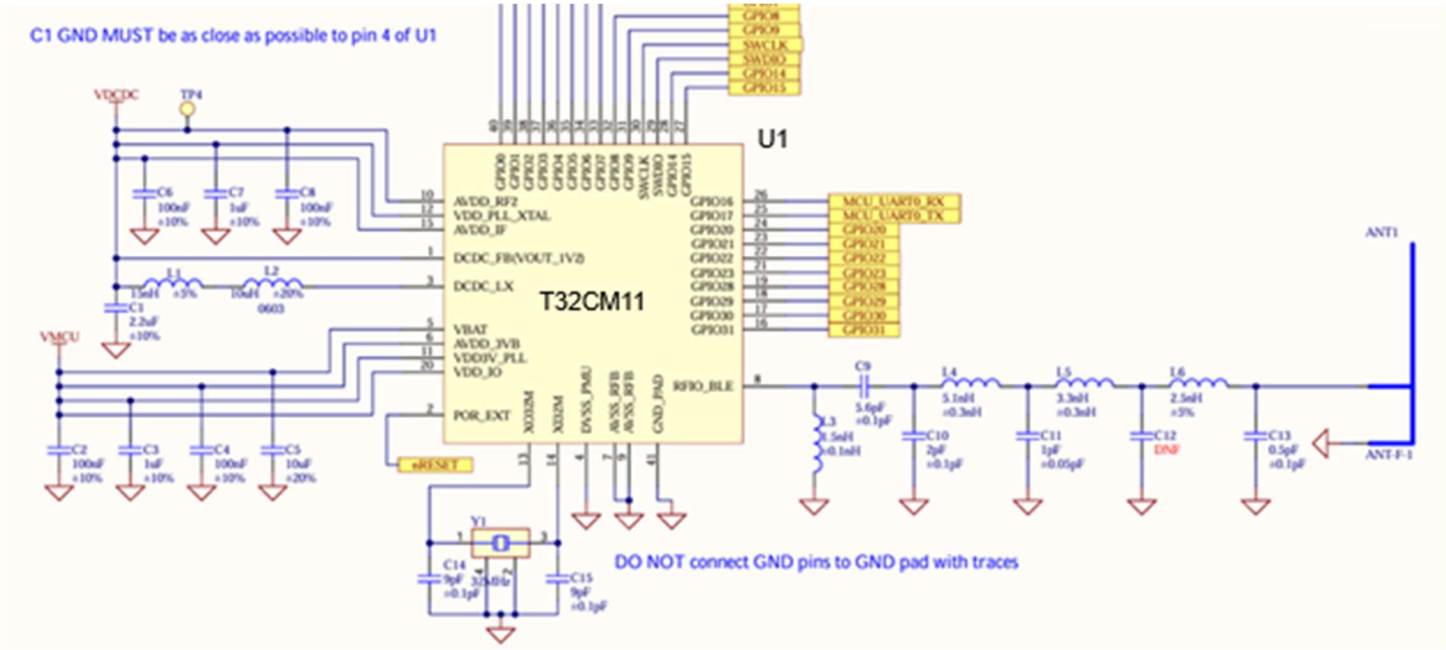
CM11 features a low-IF transmitter architecture. The transmitter is designed for high efficiency with programmable output power, allowing optimization for long-range communication while maintaining regulatory compliance. Advanced power control mechanisms enable dynamic output adjustments, balancing power consumption and link budget requirements.

12.5. Communication Subsystem

The communication subsystem is a tiny but powerful system which is optimized for handling wireless communications. It incorporates a dedicated MCU, a hardware MAC, a Modem that can support multiple wireless communication protocols. The MCU manages time-sensitive tasks associated with

wireless protocols, schedules transmission and reception timing windows. This offloads the SoC CPU, freeing up resources for user applications, and significantly reducing power consumption.

13. Typical Schematic



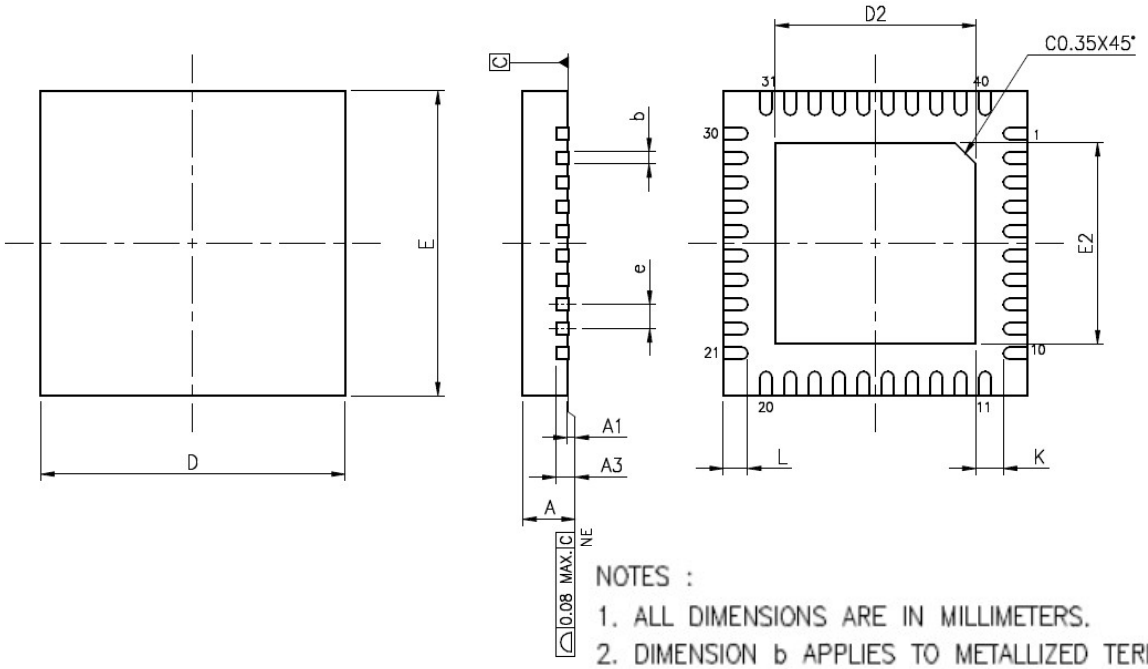
Component	Value	Function
L1	15nH	DC-DC converter
L2	10µH	DC-DC converter
C1	2.2µF	Power decoupling
Y1	32MHz	Crystal
C14, C15	9pF	32MHz Crystal loading
C2, C4, C6, C8	100nF	Power decoupling
C3, C7	1µF	Power decoupling
C5	10µF	Power decoupling

Component	Value	Function
C9	5.6pF	CM11 matching
L3	1.5nH	CM11 matching
L4	5.1nH	Low pass filter
L5	3.3nH	Low pass filter
C10	1pF	Low pass filter
C11	2pF	Low pass filter
C12	DNF	Antenna Matching Pi Network
L6	2.5nH	Antenna Matching Pi Network
C13	0.5pF	Antenna Matching Pi Network
ANT-F-1		PCB Trace Antenna

14. Package Dimensions & Outline

T32CM11 is available in 5x5mm 40-pin Quad Flat No-Lead (QFN) packaging.

5x5 40-pin QFN



NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	PACKAGE TYPE		
JEDEC	MO-220		
PKG CODE	QFN 5X5 40L		
SYMBOLS	MIN.	SYMB	MIN.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	5.00 BSC		
D2	3.25	3.30	3.35
E	5.00 BSC		
E2	3.25	3.30	3.35
L	0.35	0.40	0.45
e	0.40 BSC		
K	0.20	-	-

Note: Before soldering to a system board, the **T32CM11C10GQ40** must be baked at 125ºC more than 8 hours to eliminate moisture contamination.

15. Package Markings

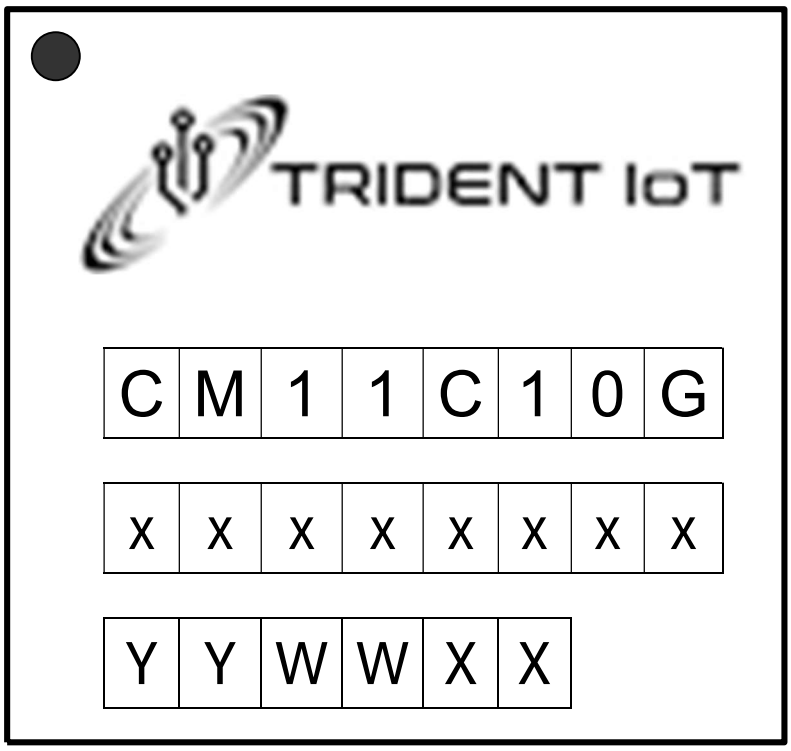


Table 16 QFN5x5-40L Package Markings

Mark Method	Laser	
Font Size	Logo：4.10mm x 1.7mm Device Number：0.55mm x 0.40mm Mfg Code & Date Code：0.45mm x 0.3mm	
Line 1 Marking	Circle = 0.35mm Diameter (Top-left justified)	Pin 1 identifier
Line 2 Marking	Device Number	CM11C10G
Line 3 Marking	XXXXXXXX = Manufacturing Code	Manufacturing Code varies by batch.
Line 4 Marking	YYWWXX YY = Year ; WW = Work Week XX = Control Code	Year & work week of the mold date. Trident IoT internal control code

16. Development Support

16.1. Developer Tools and SDK

Name	Description	Features
ELCap	ELCap is Trident IoT's Cross-Platform Command Line based development tool. This is the starting point from which to manage all device Trident SDKs. Develop, compile and flash all your Trident SoC based applications from one easy to use application.	• Command Line Interface • Enables and Orchestrates the containerized build environment within Trident SDK • VS Code Extension
Trident SDK	Software development kit for Z-Wave and Zigbee device applications using Trident IoT silicon.	• Patented Remote Command Line Interface • In-field upgrades • Bootloader • Secure boot • Signed upgrade images • FreeRTOS based applications • GCC (The GNU Complier Collection) • Integrated Build Environment.

16.2. Evaluation and Development Hardware

Part Number	Description	Features
DKN-CM11C10-02	CM11 Evaluation Board	• Integrated J-Link OB programmer & debugger • Power Supply: USB-C, CR2450 powered, ext pwr • Connectors: QWIIC, ADR Maker Shield • On Board Buttons (3), RGB Led (1) • PCB Trace Antenna
DKR-HOST-00	Main Development Board used for development and factory programming	• Integrated J-Link OB programmer & debugger • Power Supply: USB-C, CR2450 powered, ext pwr • Connectors: Radio Board Connector, QWIIC, ADR Maker Shield, Full I/O breakout for Target chip • On Board Buttons (4), LED (4)
DKR-CM11C10-25	CM11 Radio Board used for development, factory testing, and RF evaluation.	• Power Supply: via DKR-HOST-00 • Connectors: Radio Board Connector to DKR-HOST-00 • Selectable Antenna via solder bridge: PCB Trace Antenna or 50 ohm SMA connection • Footprint for External Flash

16.3. Hardware Guides

Documentation regarding implementation and validation of the T32CM11:

Document Number	Description	Features
HG-ZB-0001	Hardware Implementation Guide	• PCB Layout guidelines • Programming Footprint Reference • RF Matching, RF Calibration, TX Power Application Circuits
HG-ZB-0002	Hardware Bring Up Guide	• Hardware Design Considerations for Bring Up • Guidelines on Testing RF Performance • Guidelines on testing Electrical Performance • Guidelines on Reliability Testing

17. T32CM11 Revision History

Revision	Date	Description
A	October 28th, 2025	Release

18. Datasheet Revision History

Revision	Date	Description
-02	October 28th, 2025	• GA release Updates • Updated language • Removed Power modes that are not currently supported (deep sleep & sleep
-01	March 31, 2025	• Beta Release

19. Contact Us

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19.1. Support

Informational Links	
Support Documents	https://tridentiot.com/products/
SDK Manuals	https://tridentiot.github.io/tridentiot-sdk-docs/
Hardware Documents	https://tridentiot.com/technology/hardware/