TRIDENT IoT

T32CZ20

Sub-GHz Z-Wave RF SoC

Description

The T32CZ20 is an ultra-low power, high performance Sub-GHz wireless SoC for the Z-Wave Long Range wireless communication protocol network for automation, smart locks and smart home, and security applications. It features an integrated ARM Cortex®-M33 core with a rich set of peripherals and an integrated wireless transceiver with its own dedicated ARM Cortex®-M0+ core. It is suitable for both low-power end devices and host controllers. This makes the T32CZ20 ideal for battery-powered devices and applications where both performance and energy efficiency are essential.

The Z-Wave Long Range communication protocol propagates better through walls and has much less interference than the crowded 2.4GHz band using spread spectrum technology to transmit at much higher power and still be well within RF regulatory limits dynamically adapting RF power when needed to conserve power and has much better latency and overall downstream performance and capabilities than LoRa.

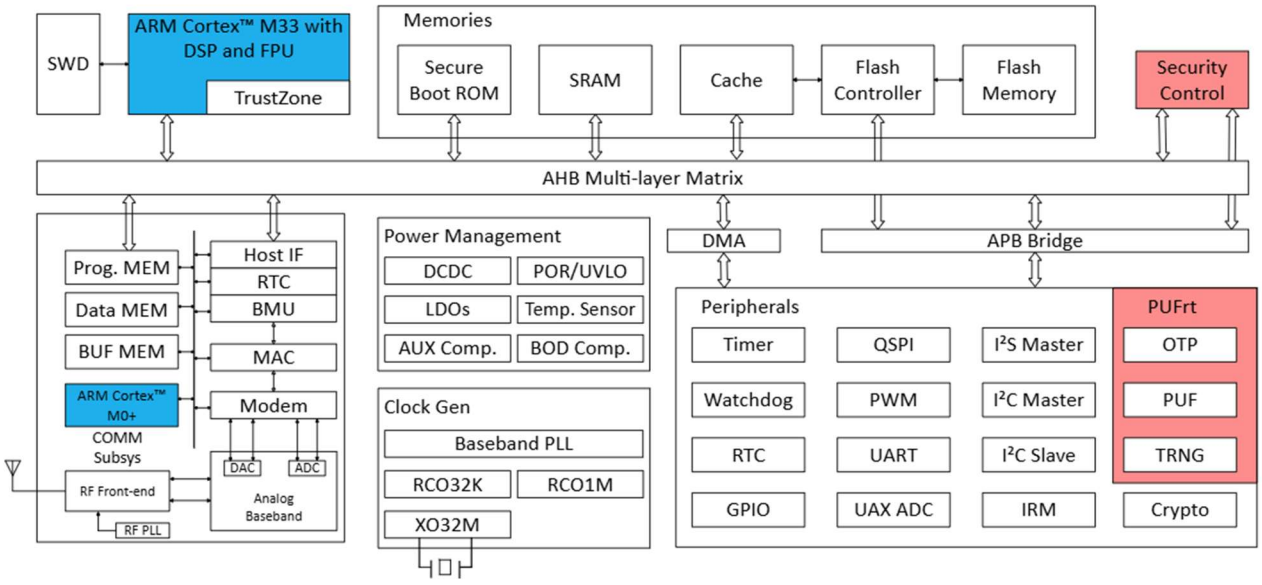


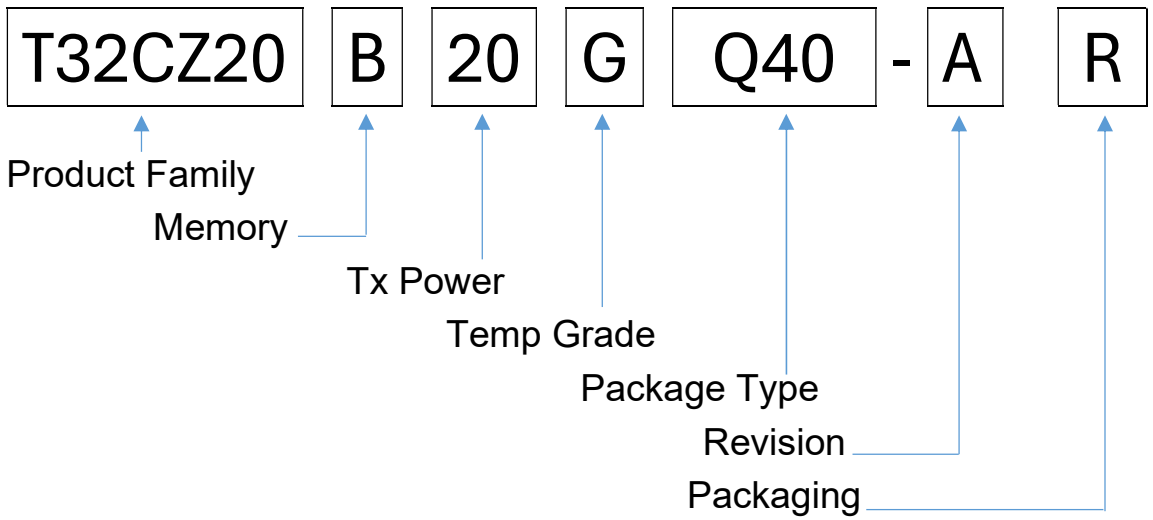
Figure 1 T32CZ20 Block Diagram

Feature List

- Transmit Power
  - +14 dBm (VDD_PA connected to VDCDC)
  - +20 dBm (VDD_PA connected to VMCU)
- Receive Sensitivity
  - -112 dBm @ 9.6 kbps FSK
  - -110 dBm @ 40 kbps FSK
  - -107 dBm @ 100 kbps GFSK
  - -108 dBm @ 100 kbps DSSS O-QPSK
- Fractional-N PLL for precise RF channel tuning
- Supported Modulations
  - (G)FSK with configurable shaping
  - DSSS O-QPSK
- Supported Data Rates
  - 9.6 kbps FSK
  - 40 kbps FSK
  - 100 kbps GFSK
  - 100 kbps DSSS O-QPSK
- Low Power Consumption
  - 5.8 mA RX current
  - 83 mA TX current @ 20 dBm
  - 25 mA TX current @ 14 dBm
  - 4.0 uA in Sleep 1
  - 1.9 uA in Sleep 2
  - 1.2 uA in Deep Sleep
- Operating Range
  - 1.8 V to 3.6 V single supply voltage
  - -40 to +85/105 ˚C
- Power Managements
  - Buck DC/DC converter
  - LDO regulators
  - Brown Out Detection
- SoC System
  - ARM Cortex®-M33 up to 64 MHz with DSP extensions and FPU
  - 288 KB SRAM (192 KB available)
  - 1 MB Flash
- SoC Peripherals
  - DMA
  - Watchdog Timer
  - RTC Timer
  - 5x 32-bit Hardware Timers
  - 5x PWM Outputs
  - 3x UART
  - 2x QSPI / SPI
  - 2x I^2C Interfaces
  - I^2C Interface as Target
  - I^2S Controller
  - Infrared Modulator
  - 22x General Purpose I/O Pins
    - 10k/100k/1M pull-ups or pull-downs
    - Hardware Debounce
    - Schmitt-Trigger Hysteresis
    - Open Drain Inputs
    - Interrupts (can wake SoC from sleep)
  - 12-bit, 350 kbps AUX ADC, up to 4 channel
  - Analogy Comparator
  - Die Temperature Sensor
- Security Features
  - Secure Boot
  - Security Control
  - True Random Number Generator
  - 3x Read Only Unique IDs / Seeds
  - Hardware Cryptographic Acceleration
  - One-Time Programmable Flash
- Package
  - QFN40 5x5 mm
  - Halogen-free, Lead-free
  - RoHS 2.0, Reach Annex 14 and 17

Ordering Information

Part Number	Package	Shipping	Minimum Order Quantity	Full Carton Quantity
T32CZ20B20GQ40-AR	QFN40 5x5mm	Reel (R)	2,500 pcs	12,500 pcs
T32CZ20B20AQ40-AR	QFN40 5x5mm	Reel (R)	2,500 pcs	12,500 pcs



Field	Values
Product Family	T32CZ20: Wireless Sub-GHz Z-Wave RF SoC
Memory	B = 1024kB
Tx Power	20 = 20dBm
Temp Grade	G = General (-40°C to 85°C) A = Automotive (-40°C to 105°C)
Package Type	Q40 = QFN 40
Revision	A = Revision A
Packaging	R = Tape & Reel T = Tray

Table of Contents

1. System Overview

1.1 Introduction

The T32CZ20 is an ultra-low power, high performance ARM® Cortex®-M33 based RF SoC supporting various protocol stacks to facilitate home & building automation, smart lighting, smart locks, sensor network, etc. applications. Designed with efficiency in mind, the “CZ20” boasts low power consumption, ensuring extended battery life for seamless operation. Its compact size and robust connectivity make it an ideal choice for integrating into a variety of devices.

Harnessing the power of ARM Cortex®-M33 and TrustZone technology, CZ20 establishes secure enclaves to safeguard critical data and processes. The integration of PUFrt®, a Physical Unclonable Function (PUF) based Root of Trust, adds an extra layer of security by leveraging unique physical variations within the chip to generate device-specific cryptographic keys, enhancing resistance to cloning. Complementing these features, the True Random Number Generator (TRNG) ensures the generation of unpredictable and truly random numbers, vital for cryptographic operations and secure communications.

1.2 SoC CPU

The Cortex®-M33 CPU is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- ✦ outstanding processing performance combined with fast interrupt handling
- ✦ efficient processor core, system and memories
  - ■ ultra-low power consumption with integrated sleep modes
- ■ Integrated security features

Table 1.2 Configurable Options of Cortex®-M33 in T32CZ20

Core Option	Description	Implementation
FPU	Floating Point Unit	YES
DSP	DSP Extension	YES
SECEXT	Security Extension	YES
SAU	Security Attribution Unit	YES (Use platform-defined security control unit instead)
NUMIRQ	Number of IRQ inputs	48
IRQLVL	Control bits of IRQ priority level	3 (8 levels)
DBGLVL	Debug level	2 (Full set of debug resources)
ITM	Instrumentation Trace Macrocell	No
ETM	Embedded Trace Macrocell	No
MTB	Micro Trace Buffer	No
WIC	Wake-up Interrupt Controller	Yes
Endianness	Memory system endianness	Little endian
JTAG/SWD	Debug interface	SWD only

1.3 Pin Assignments

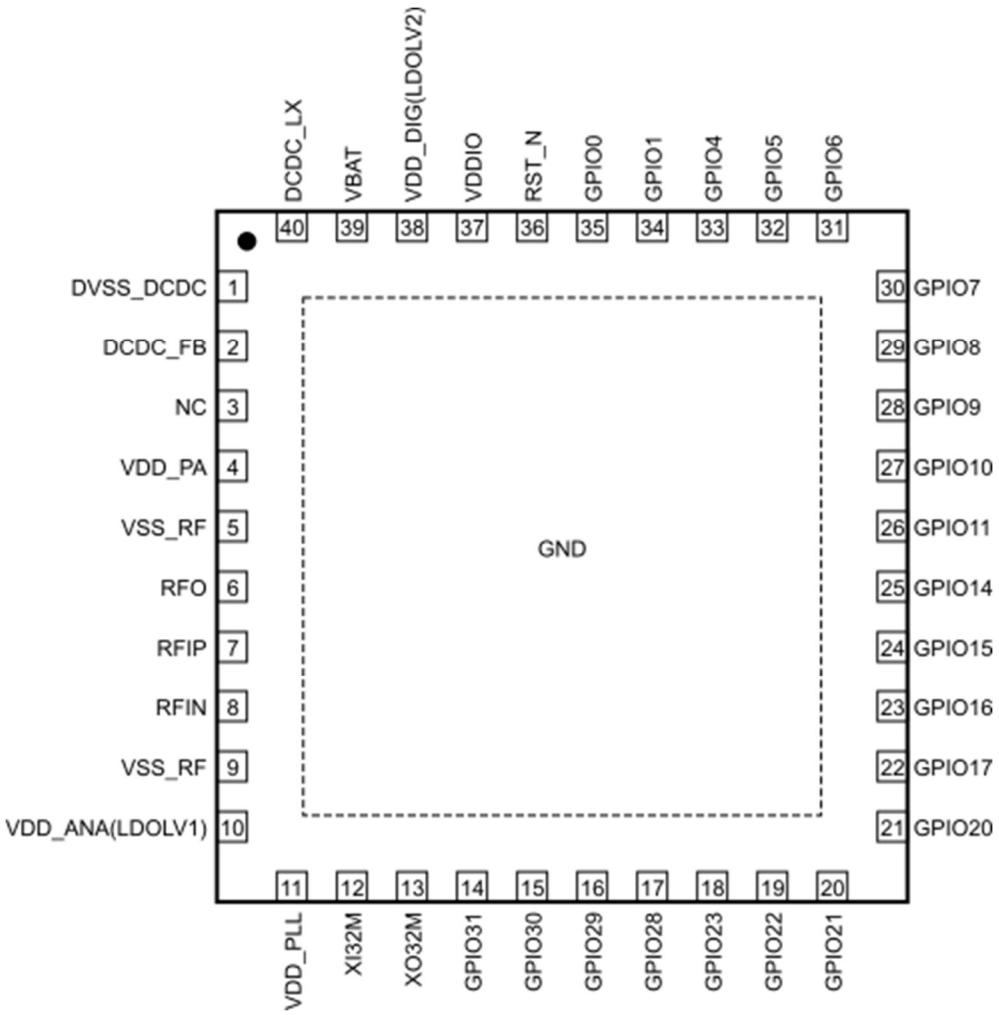


Figure 1.3 QFN40 Pinout

Table 1.3 Pin Assignments of QFN40

No.	Pin Name	Type	Description
1	DVSS_DCDC	ground	ground for PMU and DCDC
2	DCDC_FB	power	DCDC feedback input
3	NC		not connected
4	VDD_PA	power	supply for PA
5	VSS_RF	ground	ground for RF
6	RFo	RF	Sub-GHz RF output
7	RFIP	RF	Sub-GHz RF differential input P
8	RFIN	RF	Sub-GHz RF differential input N
9	VSS_RF	ground	ground for RF
10	VDD_ANA(LDOLV1)	power	supply for Analog / LDOLV1 output
11	VDD_PLL	power	supply for RF PLL
12	XI32M	analog	32MHz crystal oscillator
13	XO32M	analog	32MHz crystal oscillator
14	GPIO31	DIO	multi-function digital I/O
15	GPIO30	DIO	multi-function digital I/O
16	GPIO29	DIO	multi-function digital I/O
17	GPIO28	DIO	multi-function digital I/O
18	GPIO23	DIO	multi-function digital I/O
19	GPIO22	DIO	multi-function digital I/O
20	GPIO21	DIO	multi-function digital I/O
21	GPIO20	DIO	multi-function digital I/O
22	GPIO17	DIO	multi-function digital I/O, default UART0_TX
23	GPIO16	DIO	multi-function digital I/O, default UART0_RX
24	GPIO15	DIO	multi-function digital I/O
25	GPIO14	DIO	multi-function digital I/O
26	GPIO11	DIO	multi-function digital I/O, default ARM MCU ICE data
27	GPIO10	DIO	multi-function digital I/O, default ARM MCU ICE clock
28	GPIO9	DIO	multi-function digital I/O

No.	Pin Name	Type	Description
29	GPIO8	DIO	multi-function digital I/O
30	GPIO7	DIO	multi-function digital I/O
31	GPIO6	DIO	multi-function digital I/O
32	GPIO5	DIO	multi-function digital I/O
33	GPIO4	DIO	multi-function digital I/O
34	GPIO1	DIO	multi-function digital I/O
35	GPIO0	DIO	multi-function digital I/O
36	RST_N	DI	external reset input
37	VDD_IO	power	supply for GPIO
38	VDD_DIG(LDOLV2)	power	supply for Digital / LDOLV2 output
39	VBAT	power	supply for PMU
40	DCDC_LX	power	DCDC filter

1.4 Memory Map

Table 1.4 Memory Map

Modules	Size	Non-secure Address	Secure Address
Flash	128MB	0x00000000~0x07FFFFFF	0x10000000~0x17FFFFFF
Boot ROM	32KB	N/A	0x18000000~0x18007FFF
Reserved		0x08008000~0x0FFFFFFF	0x18008000~0x1FFFFFFF
RAM 0	32KB	0x20000000~0x20007FFF	0x30000000~0x30007FFF
RAM 1	32KB	0x20008000~0x2000FFFF	0x30008000~0x3000FFFF
RAM 2	32KB	0x20010000~0x20017FFF	0x30010000~0x30017FFF
RAM 3	32KB	0x20018000~0x2001FFFF	0x30018000~0x3001FFFF
RAM 4	32KB	0x20020000~0x20027FFF	0x30020000~0x30027FFF
RAM 5	16KB	0x20028000~0x2002BFFF	0x30028000~0x3002BFFF
RAM 6	16KB	0x2002C000~0x2002FFFF	0x3002C000~0x3002FFFF
Reserved		0x20030000~0x2003FFFF	0x30030000~0x3003FFFF
COMM Subsys RAM	96KB	0x20040000~0x20057FFF	0x30040000~0x30057FFF
Reserved		0x20030000~0x2FFFFFFF	0x30030000~0x3FFFFFFF
System Control	4KB	0x40000000~0x40000FFF	0x50000000~0x50000FFF
GPIO Control	4KB	0x40001000~0x40001FFF	0x50001000~0x50001FFF
Reserved		0x40002000~0x40002FFF	0x50002000~0x50002FFF

Modules	Size	Non-secure Address	Secure Address
Security Control	4KB	N/A	0x50003000~0x50003FFF
RTC Timer	4KB	0x40004000~0x40004FFF	0x50004000~0x50004FFF
Deep Power-down Control	4KB	0x40005000~0x40005FFF	0x50005000~0x50005FFF
Power Management	4KB	0x40006000~0x40006FFF	0x50006000~0x50006FFF
Reserved		0x40007000~0x40007FFF	0x50007000~0x50007FFF
Reserved		0x40008000~0x40008FFF	0x50008000~0x50008FFF
Flash Control	4KB	0x40009000~0x40009FFF	0x50009000~0x50009FFF
Timer 0	4KB	0x4000A000~0x4000AFFF	0x5000A000~0x5000AFFF
Timer 1	4KB	0x4000B000~0x4000BFFF	0x5000B000~0x5000BFFF
Timer 2	4KB	0x4000C000~0x4000CFFF	0x5000C000~0x5000CFFF
Slow-clock Timer 0	4KB	0x4000D000~0x4000DFFF	0x5000D000~0x5000DFFF
Slow-clock Timer 1	4KB	0x4000E000~0x4000EFFF	0x5000E000~0x5000EFFF
Reserved		0x4000F000~0x4000FFFF	0x5000F000~0x5000FFFF
Watchdog Timer	4KB	0x40010000~0x40010FFF	0x50010000~0x50010FFF
Reserved		0x40011000~0x40011FFF	0x50011000~0x50011FFF
UART 0	4KB	0x40012000~0x40012FFF	0x50012000~0x50012FFF
UART 1	4KB	0x40013000~0x40013FFF	0x50013000~0x50013FFF
Reserved		0x40014000~0x40014FFF	0x50014000~0x50014FFF
Reserved		0x40015000~0x40015FFF	0x50015000~0x50015FFF
Reserved		0x40016000~0x40016FFF	0x50016000~0x50016FFF
Reserved		0x40017000~0x40017FFF	0x50017000~0x50017FFF
I2C Slave	4KB	0x40018000~0x40018FFF	0x50018000~0x50018FFF
Reserved		0x40019000~0x40019FFF	0x50019000~0x50019FFF
COMM Subsystem	4KB	0x4001A000~0x4001AFFF	0x5001A000~0x5001AFFF
Reserved		0x4001B000~0x4001BFFF	0x5001B000~0x5001BFFF
Reserved		0x4001C000~0x4001CFFF	0x5001C000~0x5001CFFF
BOD Comparator	4KB	0x4001D000~0x4001DFFF	0x5001D000~0x5001DFFF
Analog Comparator	4KB	0x4001E000~0x4001EFFF	0x5001E000~0x5001EFFF
Reserved		0x4001F000~0x4001FFFF	0x5001F000~0x5001FFFF
QSPI 0	4KB	0x40020000~0x40020FFF	0x50020000~0x50020FFF
QSPI 1	4KB	0x40021000~0x40021FFF	0x50021000~0x50021FFF
Reserved		0x40022000~0x40022FFF	0x50022000~0x50022FFF
Reserved		0x40023000~0x40023FFF	0x50023000~0x50023FFF
IRM	4KB	0x40024000~0x40024FFF	0x50024000~0x50024FFF
UART 2	4KB	0x40025000~0x40025FFF	0x50025000~0x50025FFF
PWM	4KB	0x40026000~0x40026FFF	0x50026000~0x50026FFF
Reserved		0x40027000~0x40027FFF	0x50027000~0x50027FFF
xDMA	4KB	0x40028000~0x40028FFF	0x50028000~0x50028FFF

Modules	Size	Non-secure Address	Secure Address
DMA 0	4KB	0x40029000~0x40029FFF	0x50029000~0x50029FFF
DMA 1	4KB	0x4002A000~0x4002AFFF	0x5002A000~0x5002AFFF
I2C Master 0	4KB	0x4002B000~0x4002BFFF	0x5002B000~0x5002BFFF
I2C Master 1	4KB	0x4002C000~0x4002CFFF	0x5002C000~0x5002CFFF
I2S	4KB	0x4002D000~0x4002DFFF	0x5002D000~0x5002DFFF
Reserved		0x4002E000~0x4002EFFF	0x5002E000~0x5002EFFF
AUX ADC	4KB	0x4002F000~0x4002FFFF	0x5002F000~0x5002FFFF
Software IRQ 0	4KB	0x40030000~0x40030FFF	0x50030000~0x50030FFF
Software IRQ 1	4KB	0x40031000~0x40031FFF	0x50031000~0x50031FFF
Reserved		0x40032000~0x4043FFFF	0x50032000~0x5043FFFF
PUFrt	32KB	0x40044000~0x40047FFF	0x50044000~0x50047FFF
Crypto Accelerator	16KB	0x60000000~0x60003FFF	0x70000000~0x70003FFF

1.5 Clocks

There are several clock sources in CZ20 and they are summarized in Table 1.5-1.

Table 1.5-1 Clock Sources in T32CZ20

Clock Name	Type	Typical Frequency	Comment
XO32M	External Crystal	32 MHz	The primary oscillator for the system clock is an external 32Mhz crystal oscillator.
RCO1M	Internal RC	1 MHz	
RCO32K	Low-Frequency Internal 32kHz RC Oscillator	32 kHz	The default clock for slow-clock timers like the RTC and the primary clock after power-up until the XO32M is setup.

External 32 MHz Crystal Oscillator (XO32M)

The SoC's 32MHz oscillator is shared between the primary M33 ARM core and the transceiver, so an accurate clock signal is critical for the radio to function properly. This is the primary oscillator. The accuracy of the transmit and receive frequency of the T32CZ20 SoC is dependent on the frequency accuracy of the 32 MHz crystal oscillator that is used as the reference for the internal phase locked loop. For this reason, steps should be taken to ensure that a crystal of suitable tolerance and stability is used, and that it is loaded correctly, so this oscillator will provide an accurate reference at room temperature and over the operating temperature of the product

External 32 MHz Supported Crystals

When choosing a crystal, you should consult the crystal's datasheet for the frequency tolerances and

accuracy over temperature are good enough for your use-case. Saving money on a cheaper crystal in production can have devastating consequences in the field, so it is recommended to stick to the crystals validated by Trident-IoT.

These crystals include:

Murata P/N XRCGB32M000F1S2KR0

ECS P/N ECS-320-10-37B-CKY

Both of these crystals have a frequency tolerance of +/-10 ppm at 25C and a stability of an additional +/- 10 ppm over the operating temperature range of the crystal.

External 32 MHz Crystal Calibration

The external crystal must be calibrated during manufacturing to ensure that the PCB capacitance is accounted for so that the center frequency is within specifications. Otherwise, even if a device is working properly at room temperature, the sensitivity may be negatively affected in the field. If factory calibration of the external crystal is not able to be performed, ask Trident-IoT about a module solution such as the TZM8202 module where the crystal is pre-calibrated.

There are several approaches to maintaining proper crystal oscillator frequency calibration which offer different levels of accuracy but also require different levels of time and effort to implement.

The most accurate method is to calibrate each unit at room temperature to eliminate most of the crystal-to-crystal variation (up to +/- 10 ppm) that exists at 25C. This can be achieved by adjusting the CAL-XTAL value for minimum frequency error at room temperature and storing it inside the T32CZ20B20GQ40. This will fine tune the loading capacitance for each individual crystal on each PCB. This does improve frequency accuracy, but it also requires additional production steps and may require additional equipment.

Center Frequency without Individual PCB Calibration

Another approach is to assure that the crystal loading matches what is specified for the crystal P/N that is being used and then use the same loading capacitor value and the same CAL-XTAL setting for each unit. This will eliminate the additional calibration steps in production, but there can be up to +/- 10 ppm of unit to unit frequency variation (assuming a +/- 10 ppm crystal frequency tolerance) at 25C, in addition to the frequency variation over temperature. If this approach is taken, it is usually best to center the loading on a PCB sample with a tested crystal sample from the crystal vendor for which the exact frequency of the crystal is known. The capacitive loading should be adjusted so that the frequency of the crystal oscillator matches the vendor data for that crystal sample. This will assure that

the design is centered so the frequency error of production units will not fall far from the specified limits of the crystal. In production, each unit should still be checked to assure that the frequency is within frequency tolerance, but adjusting the loading (CAL-XTAL) value, re-checking frequency, and storing the new loading (CAL-XTAL) value is avoided.

Internal 1MHz Oscillator (RCO1M)

This is an optional internal 1MHz RC oscillator which is not used by the system by default.

Internal 32 kHz RC Oscillator (RCO32K)

The 32 kHz RC oscillator (RCO32K) is used for slow-clock timers like RTC Timer which is used for periodically waking the SoC from Sleep Modes. It is also the primary oscillator for the main core immediately after power-up until the XO32M is configured.

Baseband PLL

The baseband PLL is a phase lock loop which can be configured to run the system clock to potentially run at faster clock speeds of 36, 40, 48, or 64MHz.

1.6 Resets

The reset sources and their targets of T32CZ20 are summarized in Table 1.6-1 and graphically illustrated in Figure 1.6-1.

Table 1.6-1 Reset Sources and Targets

Reset Source	Type	Signal	Targets		
			Deep Power-down Control	RTC GPIO	All Others
VBAT	Power	vbat_por_n	O	O	O
RST_N	External pin	ext_rst_n	O	O	O
VDD_DIG	Power	vdig_por_n		O	O
Deep power-down wakeup reset	Internal event	dpd_rst_n		O	O
Deep Sleep wakeup reset	Internal event	ds_rst_n			O
Watchdog reset	Internal event	wdt_rst_n			O
Software reset	Internal event	soft_rst_n			O
MCU lockup	Internal event	mcu_lockup_n			O

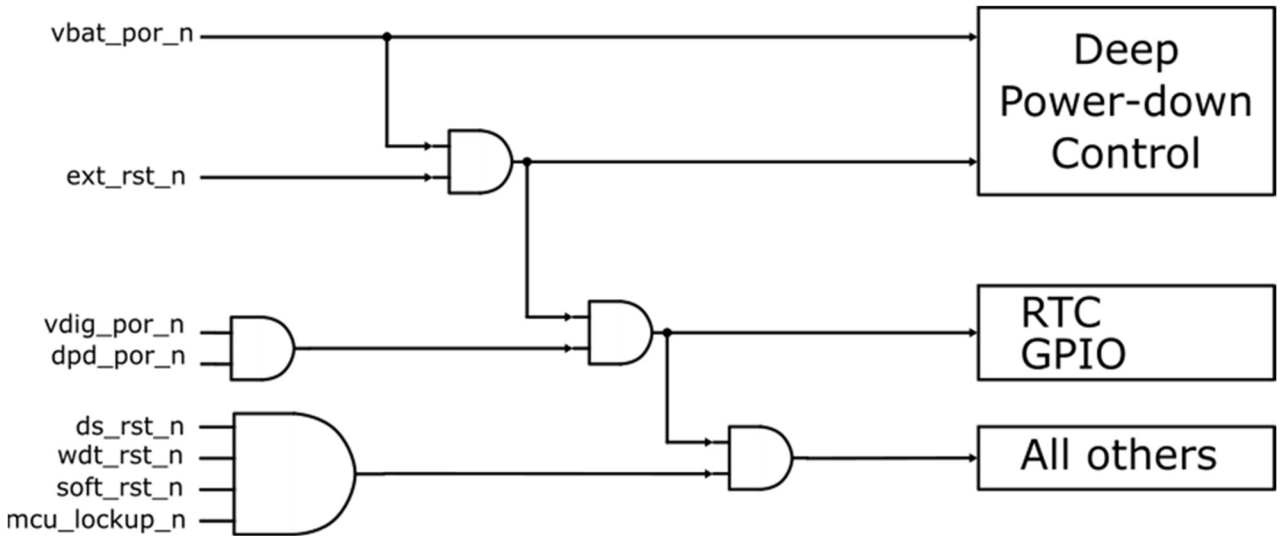


Figure 1.6-1 Reset Scheme

Power-on Reset

The power-on reset (POR) signal, vbat_por_n, is triggered when the supply voltage, VBAT, crosses the reset threshold (see Electrical Specifications). It has the highest priority over other reset signals and will reset the system as illustrated in Figure 1.6-1.

External Reset

The external reset pin, RST_N, can reset the SoC externally by asserting the pin low for at least 100us. The RST_N pin has an internal 100K ohm pull-up resistor connected, so RST_N can be left floating if not used.

Deep Power-Down Wakeup Reset

In Deep Power-Down, the SoC is powered off except the Deep Power-Down Control circuit which can reset the SoC to wake it up with the dpd_rst_n signal. (See Low-Power Modes.)

Deep-Sleep Wakeup Reset

Individual SoC components powered down during the Deep-Sleep power mode are reset by the ds_rst_n reset signal upon waking up.

Watchdog Reset

The Watchdog Timer peripheral can reset the SoC with a wdt_rst_n signal.

Software Reset

The software reset is triggered when the SYSRESETREQ bit in AIRCR register of Cortex-M33 is set. Refer to the T32CZ20 reference manual for details.

MCU Lookup

The Cortex-M33 enters a lockup state if a fault occurs when it cannot be serviced or escalated. In this situation, the processor does not execute any instructions and asserts the mcu_lockup_n signal. It will then trigger the hardware controller to reset the entire the system.

1.7 Security Control

The T32CZ20 combines the TrustZone technology of Cortex®-M33 and a custom security control mechanism to provide the ability to use secure bootloader and to partition Flash and RAM into Secure, Non-Secure Callable (NSC), and Non-Secure (NS) regions, and peripherals can also be set as either secure or non-secure.

1.8 Hardware Cryptographic Acceleration

The T32CZ20's cryptographic accelerator drastically reduces code size, memory use, execution time and therefore power use for cryptographic operations when compared to software-based solutions by supporting the following cryptographic algorithms:

- AES
  - 128-bit, 192-bit and 256-bit key length encryption/decryption
  - ECB, CBC, CTR, CMAC, CCM cipher modes
- SHA224/256
  - Can be extended to HMAC, HMAC DRBG or other
- ECC
  - 192-bit and 256-bit key length
  - Both prime field GF(p) and binary field GF(2m)
  - NIST P-192 curve (also knowns as SECP192R1)
  - NIST P-256 curve (also knowns as SECP256R1 or Prime256v1)
  - NIST B-163 curve (also knowns as SECT163R2)
  - Curve 25519
  - ECDH/ECDSA
  - ECJ-PAKE

1.9 PUFRt

T32CZ20 incorporates PUFrt® from PUFsecurity Corp. PUFrt® (Root-of-Trust) is a PUF-based (Physical-Unclonable-Function) used to establish a secure hardware root of trust, and includes a True Random Number Generator (TRNG), unique data, and a secure one-time programmable OTP key storage.

PUFrt Non-Provisioned Unique Data Source

There are 4x 256-bit read-only permanent randomized unique data available to be used as unique identifiers (UIDs) or to use as a seed for key derivation functions to generate unique encryption keys and certificates without needing to provision them in manufacturing.

PUFrt One-Time Programmable Area

The PUFrt contains two one-time programmable flash areas named OTP1 and OTP2. Each OTP page has a total size of 1K bytes, divided into 256 words: otp1_000 to otp1_255 for OTP1 and otp2_000 to otp2_255 for OTP2. Each OTP word is protected by ECC to ensure data integrity. As a result, programming the OTP requires writing the entire word, and byte-level writes are not permitted. Any unprogrammed OTP word will return 0x0 when read.

TRNG

The PUFrt's true random number generator (TRNG) is a source of cryptographic entropy, compliant with NIST SP800-90B. The TRNG utilizes four independent ring oscillators, hardware entropy health tests, and an entropy conditioning engine.

1.10 Communication Subsystem

The communication subsystem (COMM Subsys) comprises a Sub-GHz wireless transceiver, a dedicated ARM Cortex®-M0+ core with 112KB RAM, a hardware MAC, a modem, and is specifically made to handle Z-Wave and Z-Wave Long Range wireless communication protocol though other wireless protocols are technically possible.

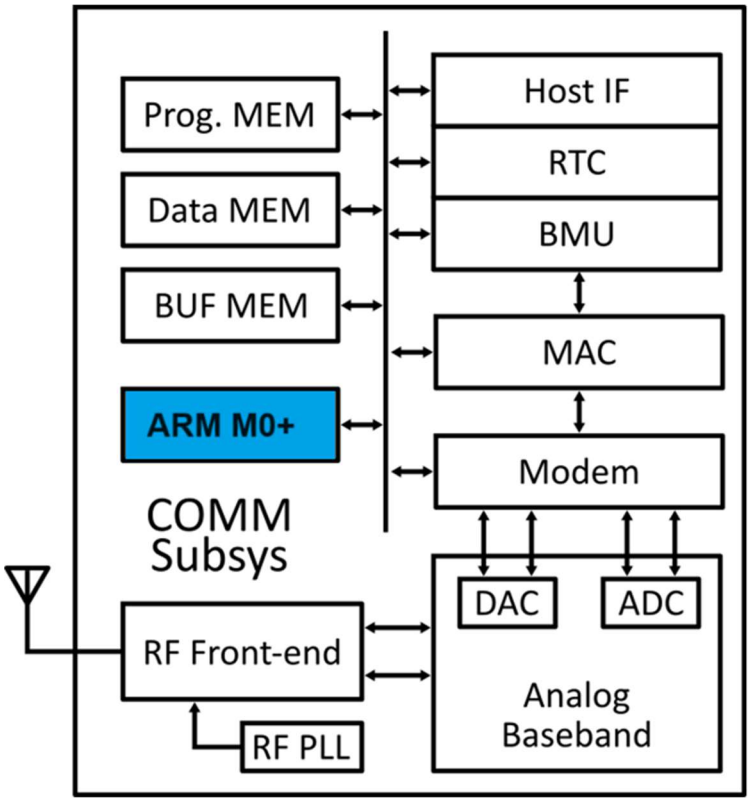


Figure 1.10-1 Block Diagram of COMM Subsystem

ARM Cortex M0+ Core

The transceiver's ARM Cortex M0+ core, serving as the radio controller, is the core component of the communication subsystem to manage time-sensitive low-level radio tasks such as scheduled transmissions and reception timing windows etc. The transceiver can be on to transmit and receive data while the main system core is idle in a low power-mode to reduce power consumption.

Buffer Memory

The communication subsystem features an 8KB buffer memory for storing transmission and reception packets. This memory is managed by the Buffer Management Unit (BMU) and is organized into multiple queues, supporting one receive queue and up to seven transmit queues. The buffer memory is shared by all queues.

Host Interface

The main system core communicates and exchanges data with the communication subsystem through the Host Interface which includes a DMA, a command and status registers with dedicated interrupts.

1.11 DMA

There are two identical DMA controllers, DMA0 and DMA1 in the T32CZ20 that can operate independently to transfer data directly from memory space to another memory space, including system memories and peripheral devices. The DMA controllers transfer data from an AHB Master write port bus to another AHB Master read port bus through the DMA Buffer.

1.12 Software IRQ

In addition to the Cortex®-M33‘s hardware interrupts, the T32CZ20 provides two additional software interrupts Software IRQ0, and Software IRQ1. Each software interrupt has 32 status bits and one additional data register that can exchange information between software tasks.

1.13 Hardware Timers

The T32CZ20 has five generic hardware timers TIMER0, TIMER1, TIMER2, TIMER3, and TIMER4. Each is a 32-bit up/down counter with a configurable pre-scaler and can be free running, periodic counting, or one-shot counter, and pulse-width modulation (PWM) output mode with configurable period and duty cycle.

1.14 Slow-clock Timer

The Slow-Clock Timer is another hardware timer that can be used as a wake-up source for the SoC when configured to use a 32kHz oscillator which is kept active while the main core is in a sleep mode.

1.15 Watchdog Timer

The Watchdog Timer is a 32-bit countdown timer with configurable pre-scaler to produce a watchdog reset signal, as well as a warning interrupt. The reset and interrupt can be enabled independently.

The Watchdog Timer also supports an additional advanced windowing to generate a reset when kicked too frequently.

1.16 RTC Timer

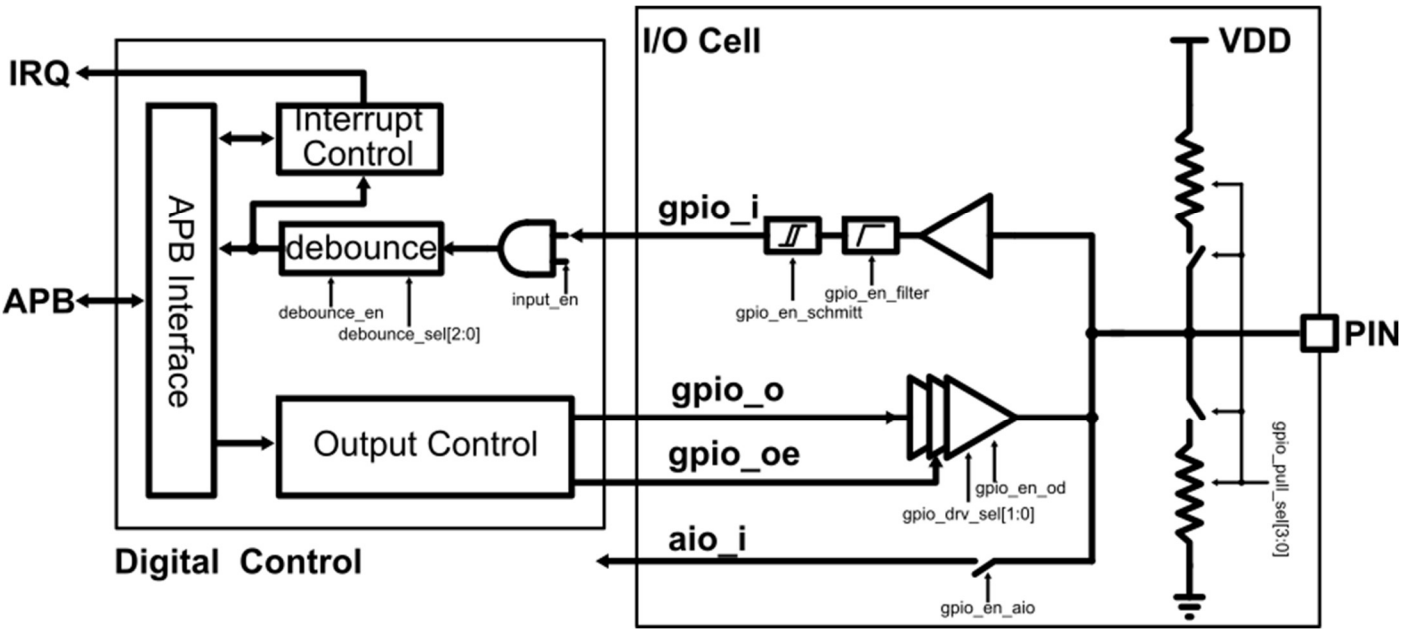
The RTC (Real Time Clock) timer provides the calendar function and maintains accurate date and time information. It enables the device to keep track of the current time and date, day of the week, month, and year. The date is encoded as represented in a binary encoding for decimal numbers, BCD, format.

It also allows the system to keep track of time for various functions such as scheduling tasks, time-stamping events, coordinating communication protocols, and maintaining accurate time for applications like alarms, timers, and logging.

1.17 GPIO

The T32CZ20's GPIO pins are highly configurable to be outputs or inputs with configurable pull-up or pull-down resistors, configurable hardware debounce, and configurable Schottky filter. Each GPIO input can be configured to have rising-edge and/or falling-edge interrupts which can also be wakeup sources in low-power modes.

Figure 1.17-1 Block Diagram of GPIO



GPIO Inputs

Each GPIO input can be individually configured to have:

- Either a pull-up or pull-down resistor of 1M/100k/10k Ohms
- Schmitt trigger for hysteresis
- Hardware Debounce
- Hardware Filter
- Falling or Risin-Edge Interrupts
- To wake up the SoC from deep sleep

1.18 GPIO Peripheral Map

GPIOx	DEFAULT	Analog	UART0	UART1	UART2	I2CM0	I2CM1	I2CS	I2S	QSPI0	QSPI1	PWMx	IRDM
0	GPIO			TX	TX	SCL	SCL	SCL	BCK	CSN1	SCK	0-4	OUT
1	GPIO			RX	RX	SDA	SDA	SDA	WCK	CSN1	CSN0	0-4	OUT
4	GPIO			TX		SCL	SCL	SCL	MCLK, SDO	DATA2, CSN1	DATA0	0-4	
5	GPIO			RX		SDA	SDA	SDA	MCLK, SDI	DATA3	DATA1, CSN1	0-4	
6	GPIO			TX	TX	SCL	SCL	SCL	SDI, BCK	SCK	SCK	0-4	
7	GPIO			RX	RX	SDA	SDA	SDA	SDO, WCK	CSN0	CSN0	0-4	
8	GPIO			RTS	TX	SCL	SCL	SCL	SDI	DATA0	DATA0, CSN1	0-4	
9	GPIO			CTS	RX	SDA	SDA	SDA	SDO	DATA1	DATA1	0-4	OUT
10	SWCLK			TX	TX	SCL	SCL		BCK	SCK, CSN1	SCK	0-4	
11	SWDIO			RX	RX	SDA	SDA		WCK	CSN0	CSN0	0-4	OUT
14	GPIO			RTS	TX	SCL	SCL	SCL	MCLK	DATA2	DATA2, CSN1	0-4	
15	GPIO			CTS	RX	SDA	SDA	SDA	MCLK	DATA3	DATA3, CSN1	0-4	
16	UART0_RX		RX	RX	RX	SCL	SCL	SCL	SDI	DATA0	DATA0	0-4	OUT
17	UART0_TX		TX	TX	TX	SDA	SDA	SDA	SDO	DATA1	DATA1	0-4	OUT
20	GPIO			RTS	TX	SCL	SCL	SCL	BCK	SCK	SCK	0-4	OUT
21	GPIO	AN0		CTS	RX	SDA	SDA	SDA	WCK	CSN0	CSN0	0-4	OUT
22	GPIO	AN1		TX	TX	SCL	SCL	SCL	SDO	DATA0	DATA0	0-4	OUT
23	GPIO	AN2		RX	RX	SDA	SDA	SDA	SDI	DATA1	DATA1	0-4	OUT
28	GPIO	AN4		TX	TX	SCL	SCL	SCL	BCK	SCK	SCK	0-4	OUT
29	GPIO	AN5		RX	RX	SDA	SDA	SDA	WCK	CSN0	CSN0	0-4	OUT
30	GPIO	AN6		RTSN	TX	SCL	SCL	SCL	SDO, MCLK	DATA0	DATA0	0-4	OUT
31	GPIO	AN7		CTSN	RX	SDA	SDA	SDA	SDI, MCLK	DATA1	DATA1	0-4	OUT

Table 1.18-1 GPIO Peripheral Availability

1.19 UART

The T32CZ20 has three UART serial peripheral communication interface peripherals with support for the standard Universal Asynchronous Receiver/Transmitter protocol: UART0, UART1, and UART2.

UART0

While UART0 is a normal UART, it lacks the optional flow control of the other two UARTs, is routable to GPIO16 and GPIO17 only, and is intended to be used for debugging purposes. We recommend connecting them to the programming connector. That said, examples may still use this UART by default, so that the development boards are easy to evaluate with UART0 being bridged over the development board's USB.

UART Features

- Baud rates up to 2Mbps
- 32-byte FIFOs
- Optional flow control signals CTSn/RTSn on UART1/2
- Optional DMA

Table 1.19-1 UART Supported Baud Rate

UART Supported Baud Rate (bps)	
2400	115200
4800	230400
9600	460800
14400	500000
19200	576000
28800	921600
38400	1000000
57600	1152000
76800	2000000

UART In Sleep

The UART peripherals can operate in low power modes, but the maximum baud rate is determined by what clock is left on. For example, by configuring the peripheral to use a 32kHz clock and limiting the baud rate to 9600bps. The clock and the peripheral on during power modes will draw extra current. See electrical characteristics for more details.

1.20 QSPI / SPI

The Quad Serial Peripheral Interface module either controls a serial data link as a primary controller or reacts to a serial data link as a target.

The core operates in various data modes (8-bit, 16-bit or 32-bit). The data is serialized and then transmitted, either LSB or MSB first, using the standard 4-wire SPI bus interface or the Quad mode bus.

The QSPI peripheral can be configured to be normal SPI interface as well.

1.21 PWM

The PWM module generates pulse width modulated signals and drives the assigned GPIOs. It supports a pulse generator with up or up-and-down counting modes. Five PWM modules can provide up to 5 PWM channels and each channel have its own individual frequency control. A DMA control is embedded in the PWM module to transfer frequency control between memory and the PWM module without CPU intervention.

1.22 I^2C Controller

The T32CZ20 has two I^2C Controller (master mode) interfaces, I2CM0, I2CM1, and one I^2C Target I2CS interface for inter-processor communication.

Each I^2C Controller supports the following features:

- Clock synchronization
- 7-bit addressing
- Transmit (9x16) and receive (8x16) buffers
- Interrupt or polling mode operation

1.23 I^2S

The I^2S is used primarily to interface to external Digital to Analog Converters (DACs) for audio applications.

The I^2S interface supports the following features:

- Support master mode only
- Support MCLK
- Support I2S, Left Justified (LJ), and Right Justified (RJ) formats
- Support 8, 16, 32 and 48 kHz sample rates
- Support 16, 24 or 32-bit data length

1.24 Infrared Modulator (IRM)

The infrared modulator is intended for devices that communicate or control via IR such television remote controls. The modulator peripheral simplifies implementing infrared protocols such as NEC, RC5, RC6, RCMM and SIRC protocols other common to TV or STB applications. It mixes a serialized data stream with a configurable PWM carrier signal.

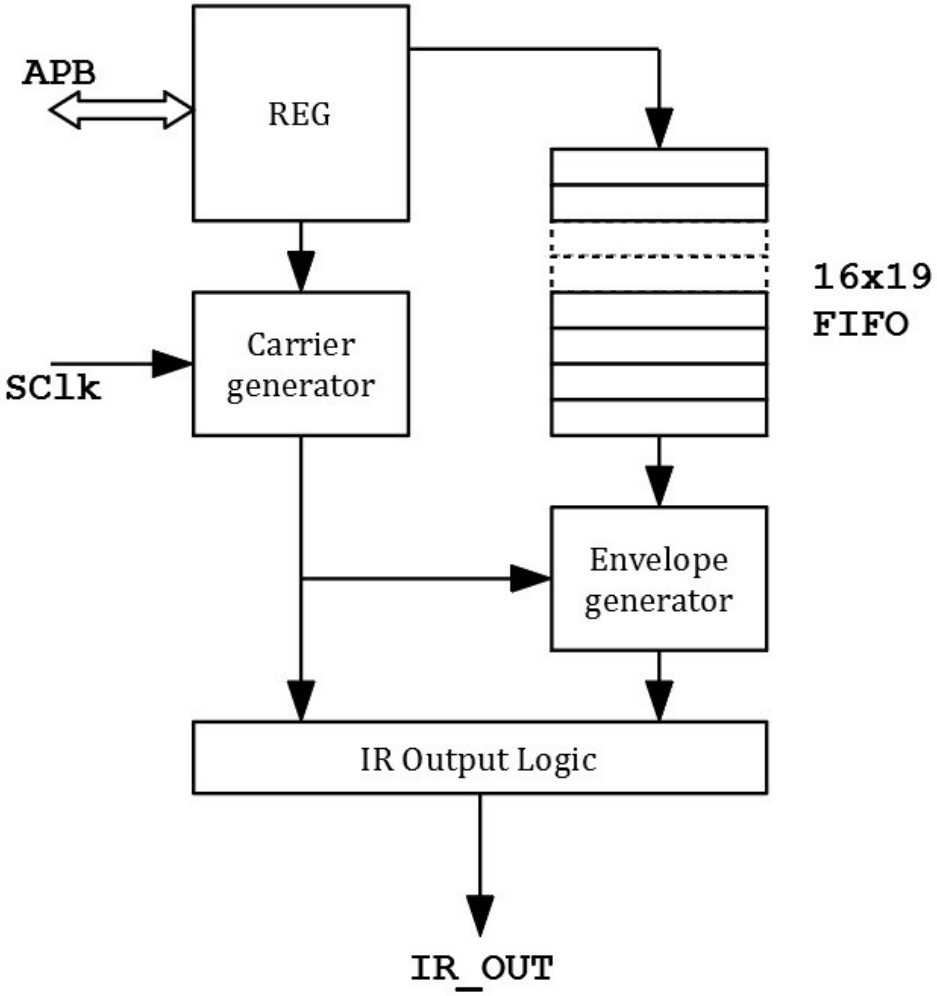


Figure 1.24-2 Block Diagram of Infrared Modulator

1.25 ADC

The T32CZ20 has a 12-bit successive approximation (SAR) analog to digital converter (ADC) peripheral used to measure voltages from external analog inputs (AIOs) or the temperature sensor or the supply voltage as a battery monitor. The AIOs are shared with GPIOs and can be configured as single or differential inputs.

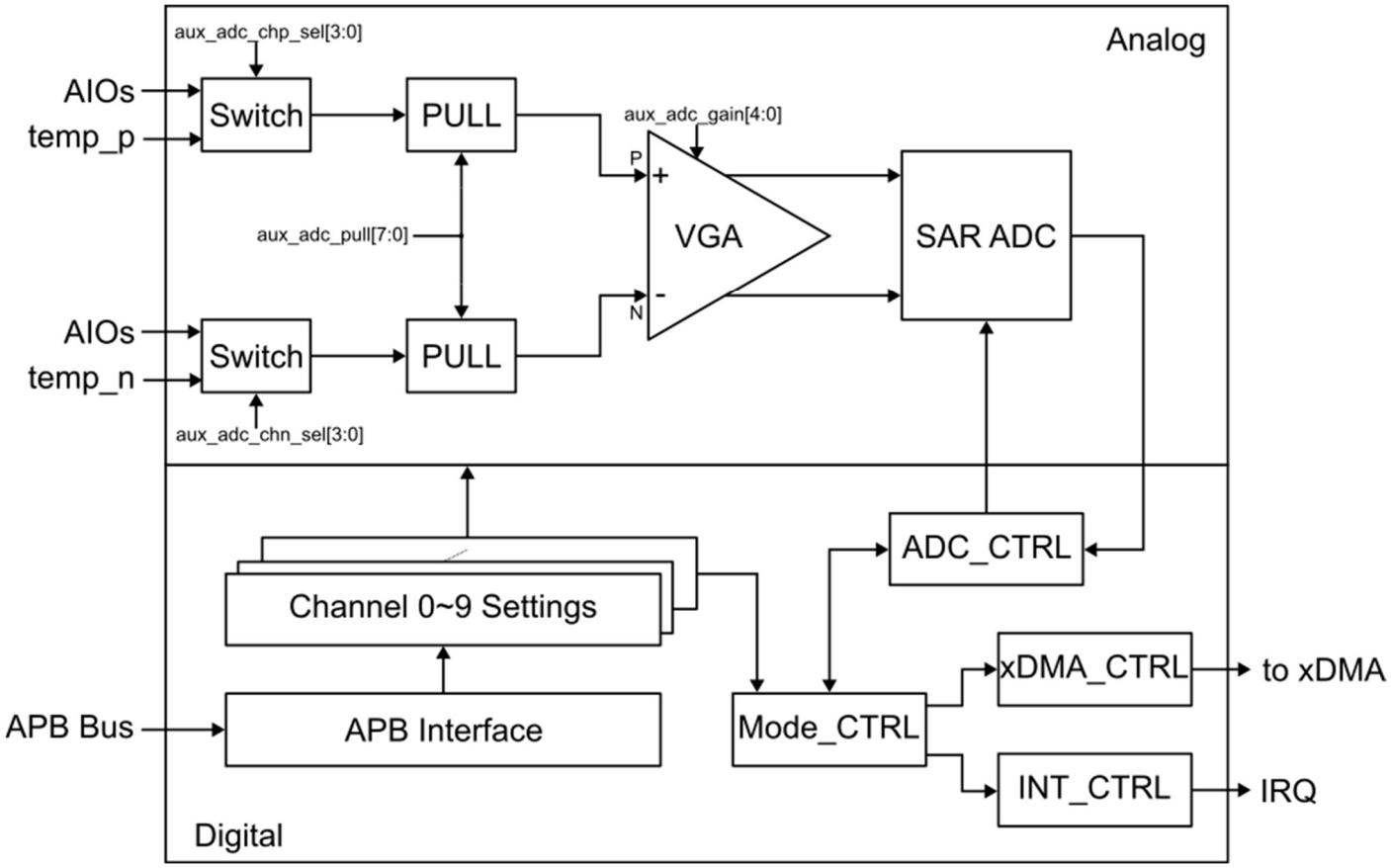


Figure 1.25-1 Block Diagram of AUX ADC

Supported Features:

- Variable Gain
- Selectable resolution of 8-bits, 10-bits, and 12-bits, and 14-bits (with oversampling)
- Single or differential AIO inputs
- One-shot, Timer, and Scan modes
- Up to 10 logical channels
- Optional DMA

1.26 Analog Comparator

The Analog Comparator can compare two analog inputs configured to be V_{in} and the reference voltage $V_{ref,}$ to output a logical high if V_{in} is greater than V_{ref}. The output of the comparator can be configured similarly to the GPIO where it can be a wake-up source, add debounce, interrupt on a rising or falling edge, or increment a counter.

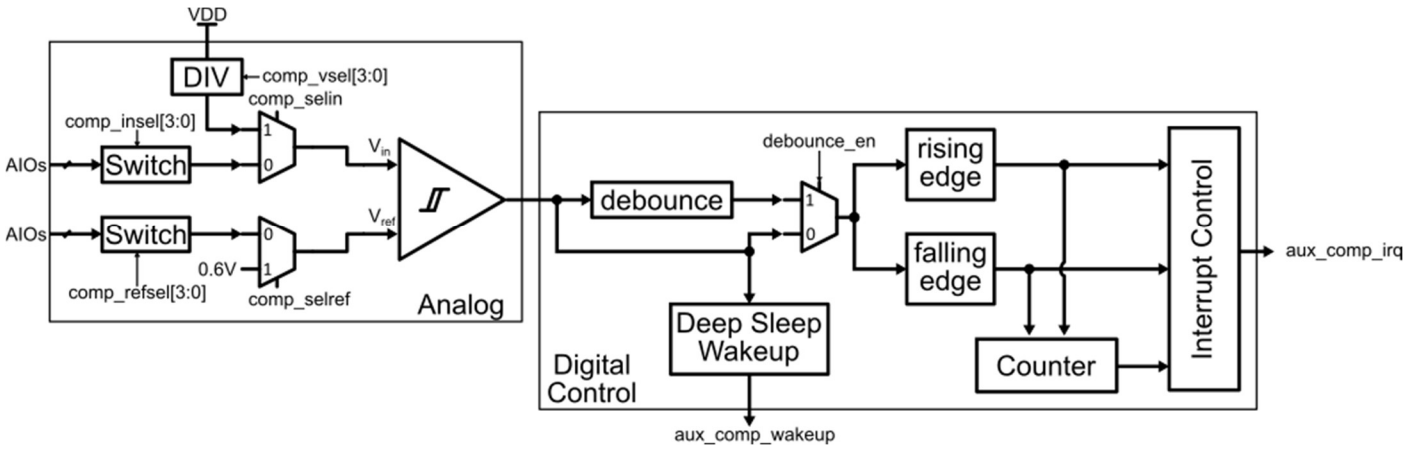


Figure 1.26-1 Block Diagram of Analog Comparator

1.27 Brown-Out Detector

The Brown-Out Detector (BOD) has a dedicated comparator where its two inputs are fixed to the divided Vdd and the bandgap reference.

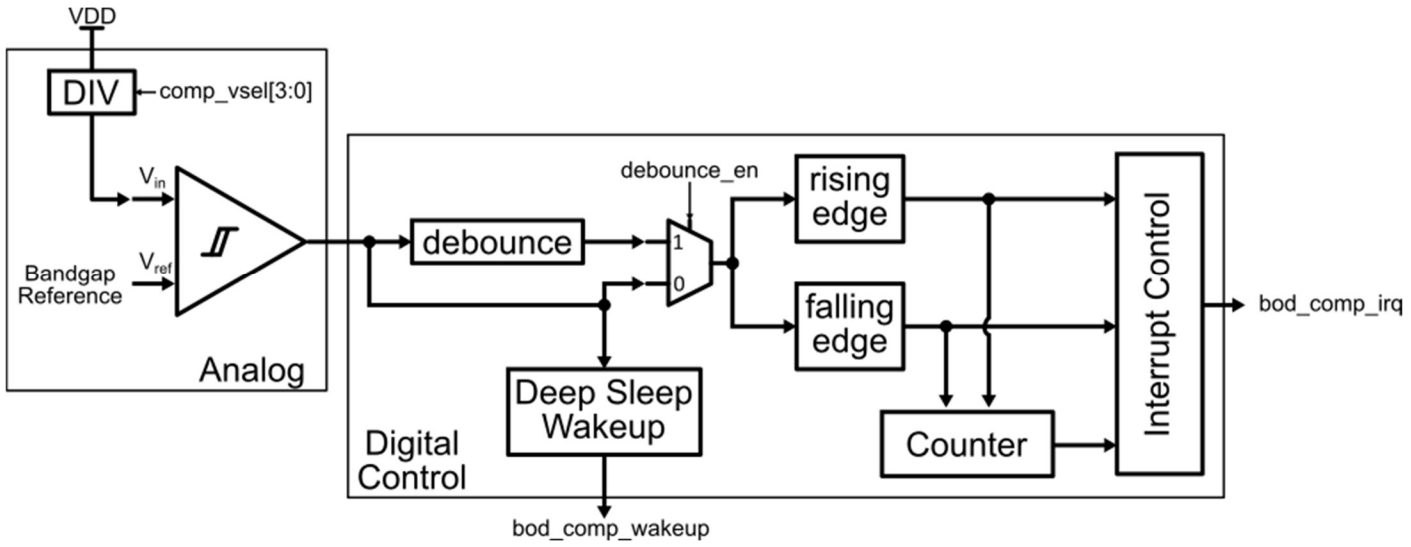


Figure 1.27-1 Block Diagram of BOD

The threshold voltage of VDD can be set from 1.8V to 2.55V with 50mV per step by the comp_vsel

register. The output of the comparator can be configured similarly to the GPIO where it can be a wake-up source, add debounce, interrupt on a rising or falling edge, or increment a counter.

1.28 Power Management

Power Structure and Connection

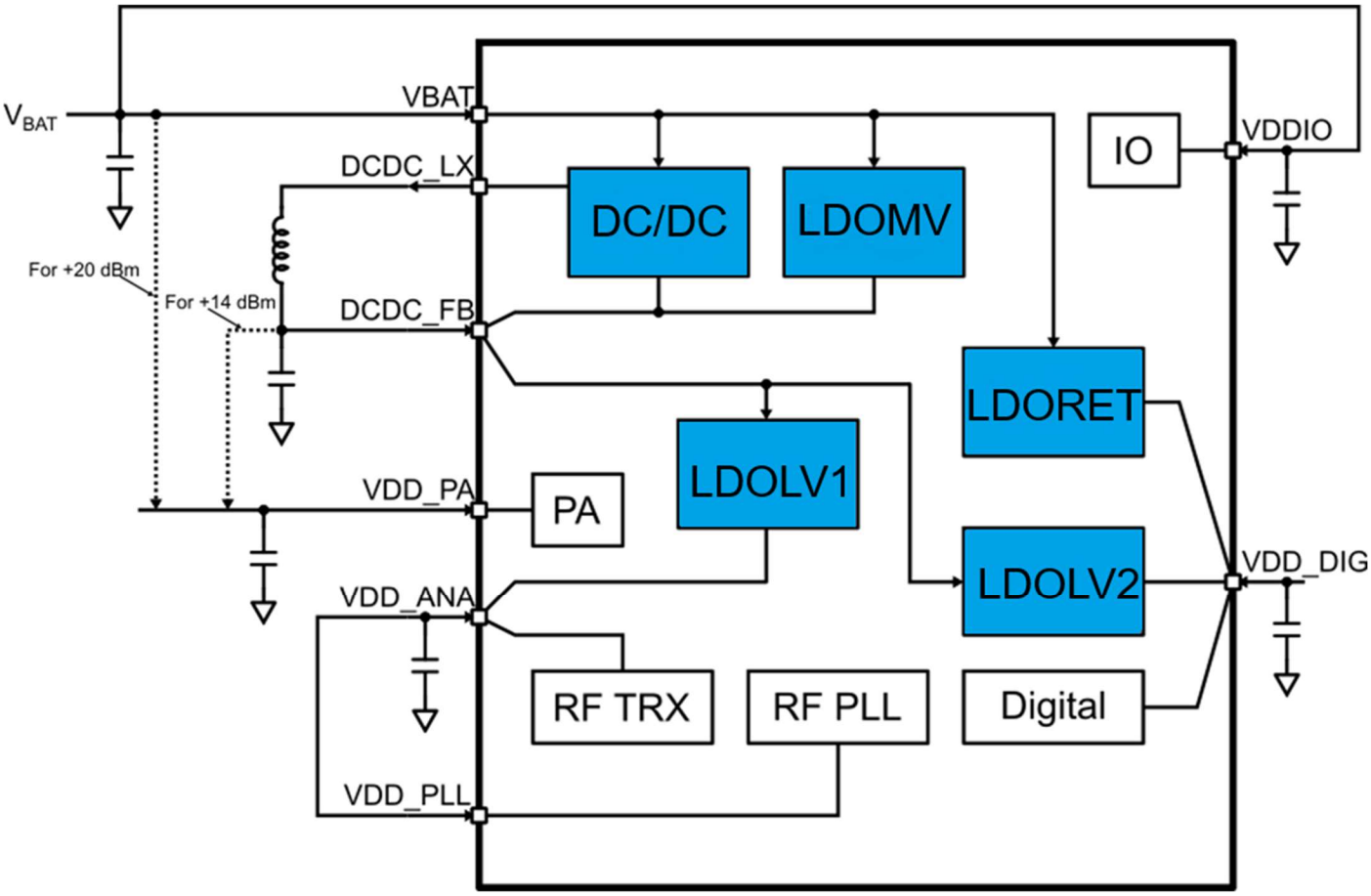


Figure 1.28-1 The Power Structure of T32CZ20

The power management contains one DC/DC Buck converter and several LDO regulators. The power structure and the power connection is illustrated in Figure 1.28-1.

Powered by V_{BAT} through the VBAT pin, the DC/DC and the LDOMV are at the first level of the power hierarchy. Either one of them will be used but not both and it will then provide the power to the next level LDO regulators, LDOLV1 and LDOLV2. Through internal and external connections, RF and analog circuits (RF TRX and RF PLL) are powered LDOLV1 and the digital circuits (Digital) are powered by LDOLV2. After power-on reset, LDOMV is turned on and DC/DC is turned off by default. Users can

switch between LDOMV and DC/DC through the software API.

The transmitter power amplifier (PA) is powered by the pin, VDD_PA. For the +14 dBm output power application, it shall be connected to DCDC_FB while for the +20 dBm one, it shall be powered by V_{BAT} directly.

The retention LDO, LDORET, is used to keep the data and states in low-power modes and all other power management components will be turned off to save the power.

Power-on Sequence

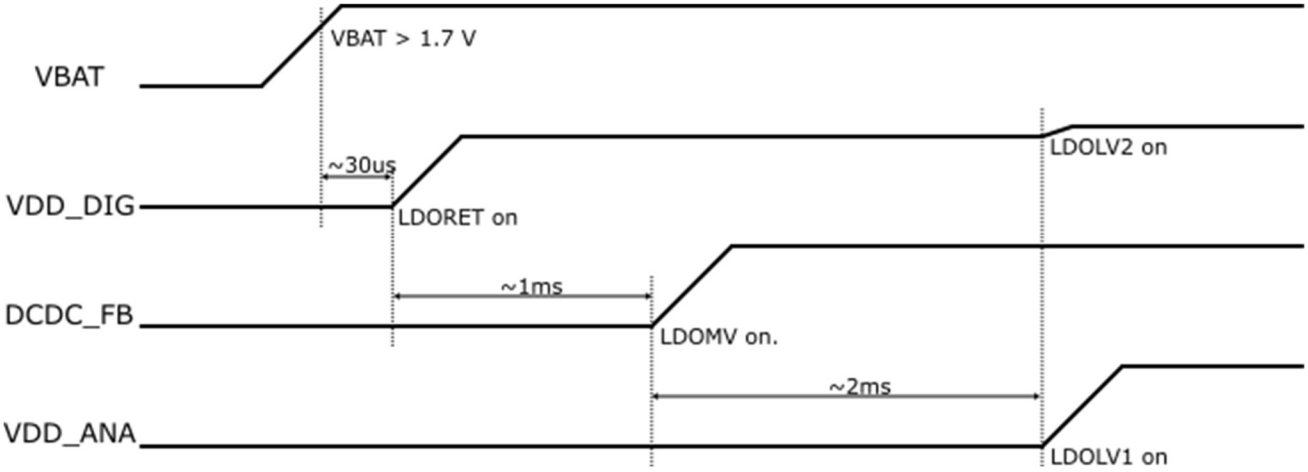


Figure 1.28-2 Power-on Sequence

1.29 Radio

Antenna Interface

The sub-GHz antenna interface of CZ20 consists of a single-ended output pin (RFO) and differential input pins (RFIP, RFIN). An external balun is required to convert the single-ended signal to a differential input. The RF matching network includes a low-pass filter designed to suppress transmitter harmonics, ensuring compliance with regulatory spectral emission limits and improving overall transmission efficiency. Proper PCB layout and impedance control are essential to minimize losses and maximize RF performance. For example, the RF trace should be kept as short as possible while ensuring it maintains a 50-ohm impedance to ensure signal integrity and reduce potential signal reflections.

RF Matching

The reference RF matching network starting values for +20 dBm output power to a SMA antenna are shown in Figure 1.29-1.

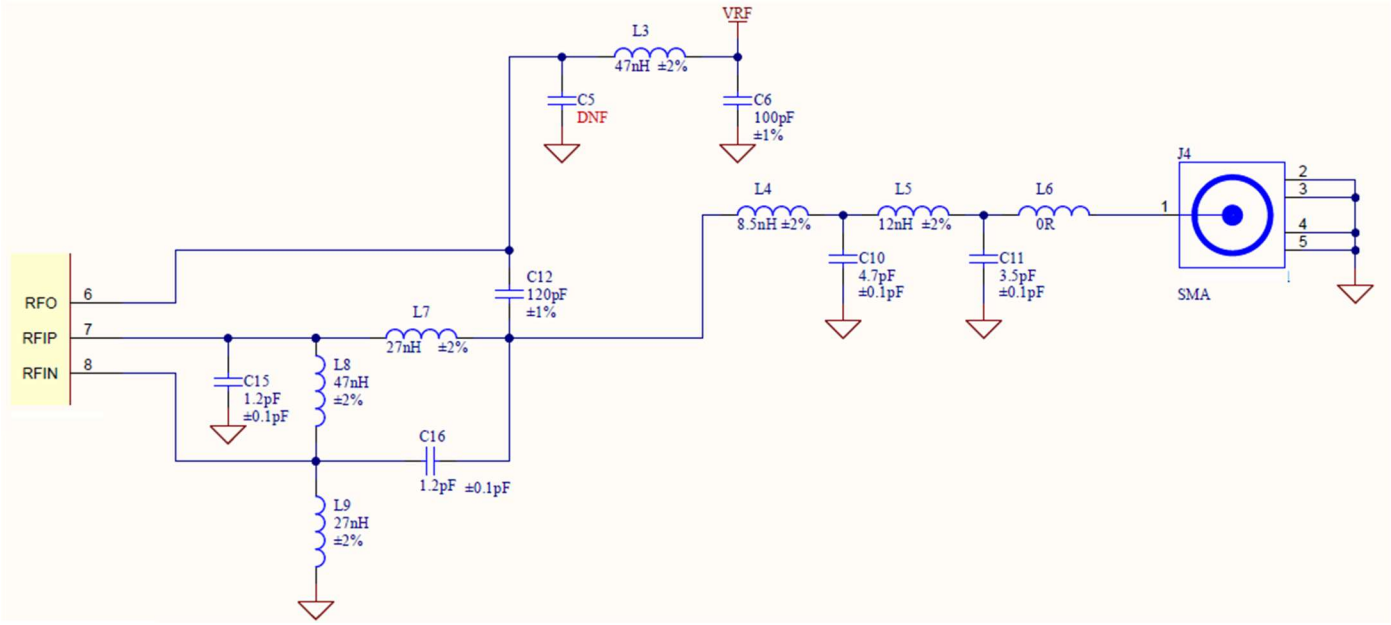


Figure 1.29-1 Reference RF Matching Network for +20 dBm Output Power

Table 1.29-1 Component Value of the +20 dBm RF Matching Network

Label	Component Value
L3, L8	47 nH ±2%
L7, L9	27 nH ±2%
L4	8.5 nH ±2%
L5	12 nH ±2%
C15, C16	1.2 pF ±0.1pF
C12	120 pF ±1%
C6	100 pF ±1%
C10	4.7 pF ±0.1pF
C11	3.5 pF ±0.1pF
L6	0 ohm resistor
C5	DNF

The reference RF matching network starting values for +20 dBm output power to a PCB Trace antenna power are shown in Figure 1.29-2.

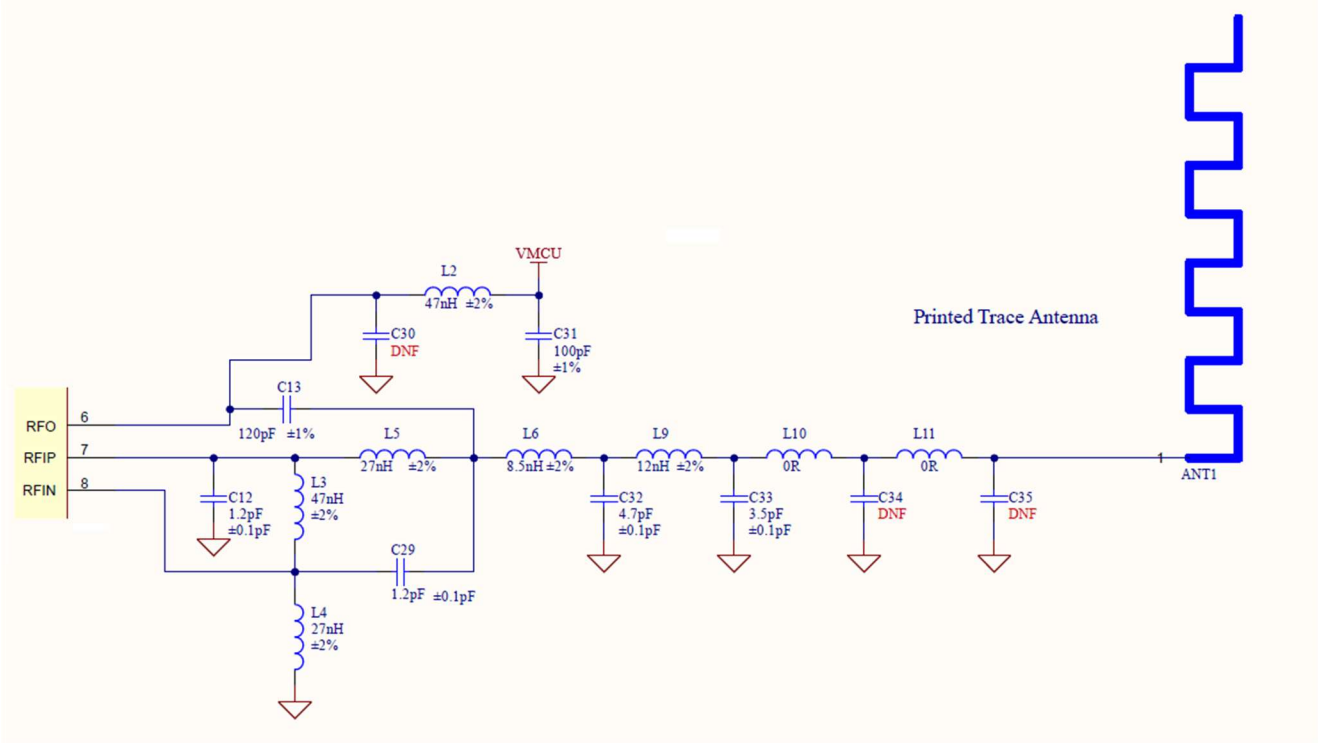


Figure 1.29-2 Reference RF Matching Network for +20 dBm Output Power

Table 1.29-2 Component Value of the +20 dBm RF Matching Network

Label	Component Value
L2, L3	47 nH ±2%
L4, L5	27 nH ±2%
L6	8.5 nH ±2%
L9	12 nH ±2%
C12, C29	1.2 pF ±0.1pF
C13	120 pF ±1%
C31	100 pF ±1%
C32	4.7 pF ±0.1pF
C33	3.5 pF ±0.1pF
L10, L11	0 ohm resistor
C30, C34, C35	DNF

These component values should be suitable for most applications assuming layout recommendations are followed, but it should be noted that the antenna matching components C34, L11 and C35 will vary depending on the feed point impedance of the antenna and will most likely need to be changed.

Power Amplifier

The single power amplifier can support the maximum output power of +20 dBm or +14 dBm depending on the voltage connected to its power pin, VDD_PA. This is because the PA output power is proportional to the square of the supplying voltage and when the voltage of VDD_PA is halved, the output power will be reduced by 6 dB. Users shall decide which maximum output power will be supported and route VDD_PA to the proper voltage source on the PCB level. Table 1.29-3 lists VDD_PA voltages required for the +20 and +14 dBm maximum output power respectively.

Table 1.29-3 VDD_PA Voltages and Tx Current for +14 and +20 dBm Maximum Output Power

Maximum Output Power	VDD_PA Voltage	Tx Current
+20 dBm	3.3 V, from VBAT	83 mA
+14 dBm	1.6 V, from DCDC	25 mA

The Fractional-N RF PLL

The RF PLL is used to generate the desired LO frequency in receiving and the RF channel frequency in transmitting. It utilizes the delta-sigma fractional-N architecture that can provide finer frequency resolution, reduced phase noise and spurs, faster lock time, lower jitter and power efficiency.

Receiver Architecture

- Enhanced sensitivity and selectivity Low-IF receiver
- Low-Noise Amplifier (LNA)
- Low-Noise High Linearity Quadrature Down-Conversion Mixer
- Automatic Gain Control (AGC)
- Real-time Received Signal Strength Indicator (RSSI) for adaptive power control and clear-channel assessment.

Transmitter Architecture

- Direct-Conversion Transmitter
- Configurable Modulation such as (G)FSK with Spectral Shaping and DSSS O-QPSK with Raised Cosine Shaping
- Programmable Output Power

1.30 Low Power Modes

The supported low-power modes are summarized in the table below. The SoC will perform a reset waking from Deep Sleep.

Table 1.30-1 Summary of Low-power Modes

Power Modes	Active LDOs	Active Clocks	CPU State	Memory	Wakeup
Normal	MV DCDC/(LDO)* LV LDO Retention LDO	RCO32K XO32M (Baseband PLL) (RC01M)	Active WFI/WFE	On	Interrupts
Sleep	Retention LDO	RCO32K (RC01M)	WFI/WFE	On	Interrupts
Deep Sleep	Retention LDO	Off/(RCO32K)	Off	1024 Bytes	GPIO (RTC timer)

**Items inside ( ) are optional.*

Power Domains of Peripherals

The peripherals are partitioned into four power domains. Table 1.30-2 shows the default behaviors of each peripheral power domain in each low-power mode.

Table 1.30-2 Power Domains of Peripherals

Power Domain	Peripherals	Sleep	Deep Sleep
Always on	RTC Timer GPIO Control Watchdog Timer Analog Comparator Brown-Out Detector	On	On
Peripherals 1	Cortex-M33 Flash Control UART 0 I2C Slave Slow-clock Timer 0/1 Security Control	On	Off
Peripherals 2	PWM DMA 0/1 UART 2 QSPI 0/1 Crypto Accelerator I2C Master 0 I2C Master 1 AUX ADC IRM PUFrt	Off	Off
Peripherals 3	Cache Control UART 1 Timer 0/1/2 FPU of Cortex-M33 DBG of Cortex-M33	Off	Off

Be aware of peripherals in Peripherals 2 Power domain. Because those peripherals are powered off in Sleep mode by default, their internal states are reset to the default values after waking up from Sleep mode. It is suggested to run initialization procedures of the peripheral every time it is used.

2. Electrical Specifications

2.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
PMU supply voltage	V_{BATMAX}	At pin VBAT	-0.3	3.9	V
IO supply voltage	V_{IOMAX}	At pin VDD_IO	-0.3	3.9	V
PA supply voltage	V_{PAMAX}	At pin VDD_PA	-0.3	3.9	V
Analog/RF supply voltage	V_{ANAMAX}	At pin VDD_ANA/VDD_PLL	-0.3	1.26	V
Digital supply voltage	V_{DIGMAX}	At pin VDD_DIG	-0.3	1.26	V
DC voltage for GPIOs	$V_{DCIOMAX}$		-0.3	V_{IO}+0.3	V
Storage temperature	T_{STG}		-50	150	˚C
Junction temperature	T_J			125	˚C
Moisture sensitivity level	MSL			3	

2.2 ESD Rating

Parameter	Symbol	Condition		Value	Unit
Human body model	HBM	JEDEC JS-001		±2000	V
Charged device model	CDM	JEDEC JS-002		±300	V

2.3 Thermal Characteristics

Parameter	Symbol	Condition		Value	Unit
Thermal resistance, junction to ambient	Θ_{JA}			47	˚C/W
Thermal resistance, junction to case	Θ_{JC}			4.5	˚C/W

2.4 General Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating ambient temperature	T_A		-40	25	85/105*	˚C
PMU supply voltage	V_{BAT}		1.8	3.3	3.6	V
IO supply voltage	V_{IO}		1.8	3.3	3.6	V
PA supply voltage	V_{PA}	+20 dBm		3.3		V
		+14 dBm		1.6		V
Analog/RF supply voltage	V_{ANA}	Include VDD_ANA and VDD_PLL pins.		1.1		V
Digital supply voltage	V_{DIG}			1.1		V

*Max operating temperature 85°C for T32CZ20B20**G**, 105°C for T32CZ20B20**A**

2.5 Boot Time

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Boot time from Power-off	$T_{BOOT-OFF}$	From power-off to CPU run		13.5		ms
Boot time from Deep-power down	$T_{BOOT-DPD}$	From deep-power down to CPU run		13.5		ms
Boot time from Deep-sleep	$T_{BOOT-DS}$	From deep-sleep to CPU run		4.0		ms

2.6 Wakeup and Sleep Time

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Wakeup from Deep Sleep*	$T_{WAKE-DS}$	Code execution from Boot ROM		2.45		ms
		Code execution from Flash		2.75		ms
Wakeup from Sleep**	$T_{WAKE-SP}$	Code execution from Flash. Divided-by-2 is enabled for rco32k.		1.94		ms
		Code execution from Flash. Divided-by-2 is disabled for rco32k.		2.75		ms
Entry time to Deep Sleep	T_{GO-DS}			240		µs
Entry time to Sleep	T_{GO-SP}	Divided-by-2 is enabled for rco32k.		197		µs
		Divided-by-2 is enabled for rco32k.		103		µs

(*)Wakeup sources from Deep Sleep can be either GPIO or RTC.
(**)Wakeup sources from Sleep can be any available interrupt.

2.7 Clock Specifications

32 MHz Crystal Oscillator

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency	F_{XO32M}			32		MHz
Equivalent series resistance	ESR				60	Ω
Load capacitance	C_L			8		pF

32 kHz RC Oscillator

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency	F_{RCO32K}			32		kHz
Calibrated frequency variation				±500		ppm
Start-up time	T_{START}			500		µs

2.8 Current Consumption

Unless otherwise indicated, typical conditions are: V_{BAT} = 3.3 V. T_A = 25 ˚C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Current consumption of MCU per MHz	I_{MCU}	All peripherals are disabled and DCDC is used.		54.9		µA/MHz
Current consumption in Sleep 1 mode	I_{SLP1}	SoC system is in Sleep mode. Communication sub-system is in Sleep mode and wireless links are maintained. Wake up by GPIO or Timer. Slow clock is 16 kHz.		4.0		µA
		SoC system is in Sleep mode. Communication sub-system is in Sleep mode and wireless links are maintained. Wake up by GPIO or Timer. Slow clock is 32 kHz.		4.2		µA
Current consumption in Sleep 2 mode	I_{SLP2}	SoC system is in Sleep mode. Communication sub-system is in Deep Sleep mode and wireless links are lost. Wake up by GPIO or Timer. Slow clock is 16 kHz.		1.9		µA
		SoC system is in Sleep mode. Communication sub-system is in Deep Sleep mode and wireless links are lost. Wake up by GPIO or Timer. Slow clock is 32 kHz.		2.0		µA
Current consumption in Deep Sleep mode	I_{DSLP}	Wake up by GPIO only without retention memory. RC oscillator is off.		1.2		µA
		Wake up by GPIO only with 16 KB retention memory. RC oscillator is off.		1.3		µA
Current consumption in Deep Power-down mode	I_{DPD}	Wake up by GPIO only.		0.5		µA

2.9 Flash Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Flash supply voltage	VDD_{FLASH}		1.65		3.6	V
Flash data retention	RET_{FLASH}			20		years
Flash erase/program cycles	EP_{FLASH}		100,000			cycles
Flash program time	T_{PRG}	one byte		65	240	µ
		one page (256 bytes)		1	8	ms
Flash erase time	T_{ERASE}	4 KB		100	800	ms
		32 KB		0.3	3	s
		64 KB		0.5	6	s
		Whole chip (1MB)		5	30	s
Flash program current	I_{PRG}			15	30	mA
Flash program time	I_{ERASE}			15	30	mA

2.10 Sub-G RF Transceiver Characteristics

Unless otherwise indicated, typical conditions are: V_{BAT} = 3.3 V. T_A = 25 ˚C. V_{ANA} = 1.1 V with DC/DC enabled.

Transmit Characteristics @ 14 dBm Output Power at 908/912/916/920 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RF output power	P_{OUT}	V_{PA} = 1.6 V	-20		+14	dBm
Operating frequency	F_{OPT}	R1: FSK, 9.6 kbps and R2: FSK, 40 kbps		908		MHz
		R3: GFSK, 100 kbps		916		MHz
		LR: DSSS O-QPSK, 100 kbps		912		MHz
		LR: DSSS O-QPSK, 100 kbps		920		MHz
Frequency deviation	F_{DEV}	R1: FSK, 9.6 kbps and R2: FSK, 40 kbps	32	40	48	kHz
		R3: GFSK, 100 kbps	46.4	58	69.6	kHz
Offset EVM	EVM	LR: DSSS O-QPSK, 100 kbps	2	2.5	3	%

Transmit Characteristics @ 20 dBm Output Power at 908/912/916/920 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RF output power	P_{OUT}	V_{PA} = 3.3 V	-10		+20	dBm
Operating frequency	F_{OPT}	R1: FSK, 9.6 kbps and R2: FSK, 40 kbps		908		MHz
		R3: GFSK, 100 kbps		916		MHz
		LR: DSSS O-QPSK, 100 kbps		912		MHz
		LR: DSSS O-QPSK, 100 kbps		920		MHz
Frequency deviation	F_{DEV}	R1: FSK, 9.6 kbps and R2: FSK, 40 kbps	32	40	48	kHz
		R3: GFSK, 100 kbps	46.4	58	69.6	kHz
Offset EVM	EVM	LR: DSSS O-QPSK, 100 kbps	2	2.5	3	%

Receive Characteristics at 908/912/916/920 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Sensitivity	SENS	R1: FSK, 9.6 kbps		-112		dBm
		R2: FSK, 40 kbps		-110		dBm
		R3: GFSK, 100 kbps		-107		dBm
		LR: DSSS O-QPSK, 100 kbps		-108		dBm
Adjacent interference rejection, ±1 MHz	$C/I_{ADJ(\pm 1M)}$	R1: FSK, 9.6 kbps		-48		dB
		R2: FSK, 40 kbps		-45		dB
		R3: GFSK, 100 kbps		-42		dB
Adjacent interference rejection, ±2 MHz	$C/I_{ADJ(\pm 2M)}$	R1: FSK, 9.6 kbps		-58		dB
		R2: FSK, 40 kbps		-55		dB
		R3: GFSK, 100 kbps		-52		dB
		LR: DSSS O-QPSK, 100 kbps		-49		
Out-of-band blocking, ±5 MHz	OOB_{5M}	R1: FSK, 9.6 kbps		-65		dB

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		R2: FSK, 40 kbps		-62		dB
		R3: GFSK, 100 kbps		-59		dB
		LR: DSSS O-QPSK, 100 kbps		-54		dB
Out-of-band blocking, ±10 MHz	OOB_{10M}	R1: FSK, 9.6 kbps		-67		dB
		R2: FSK, 40 kbps		-64		dB
		R3: GFSK, 100 kbps		-61		dB
		LR: DSSS O-QPSK, 100 kbps		-59		dB
RSSI			-100		0	
Note: All data is under the condition of full calibrations.						

3. Application Circuits

3.1 Application Circuit for +14 dBm Transmit Power

VDCDC = 1.6VDC from DCDC of CZ20

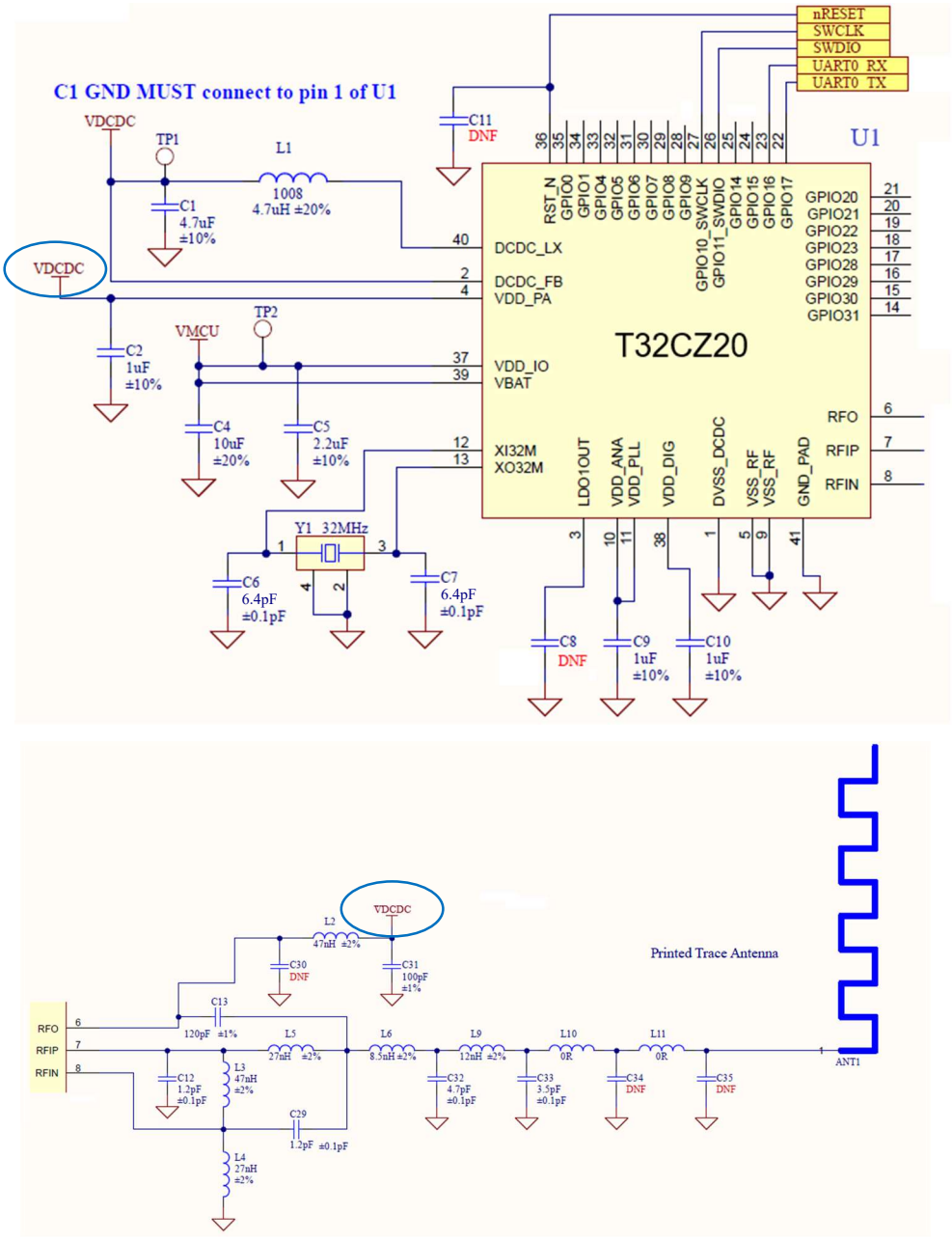


Figure 3.1-1 Application Circuit for +14 dBm Transmit Power

3.2 Application Circuit for +20 dBm Transmit Power

VMCU = 3.3VDC supply voltage

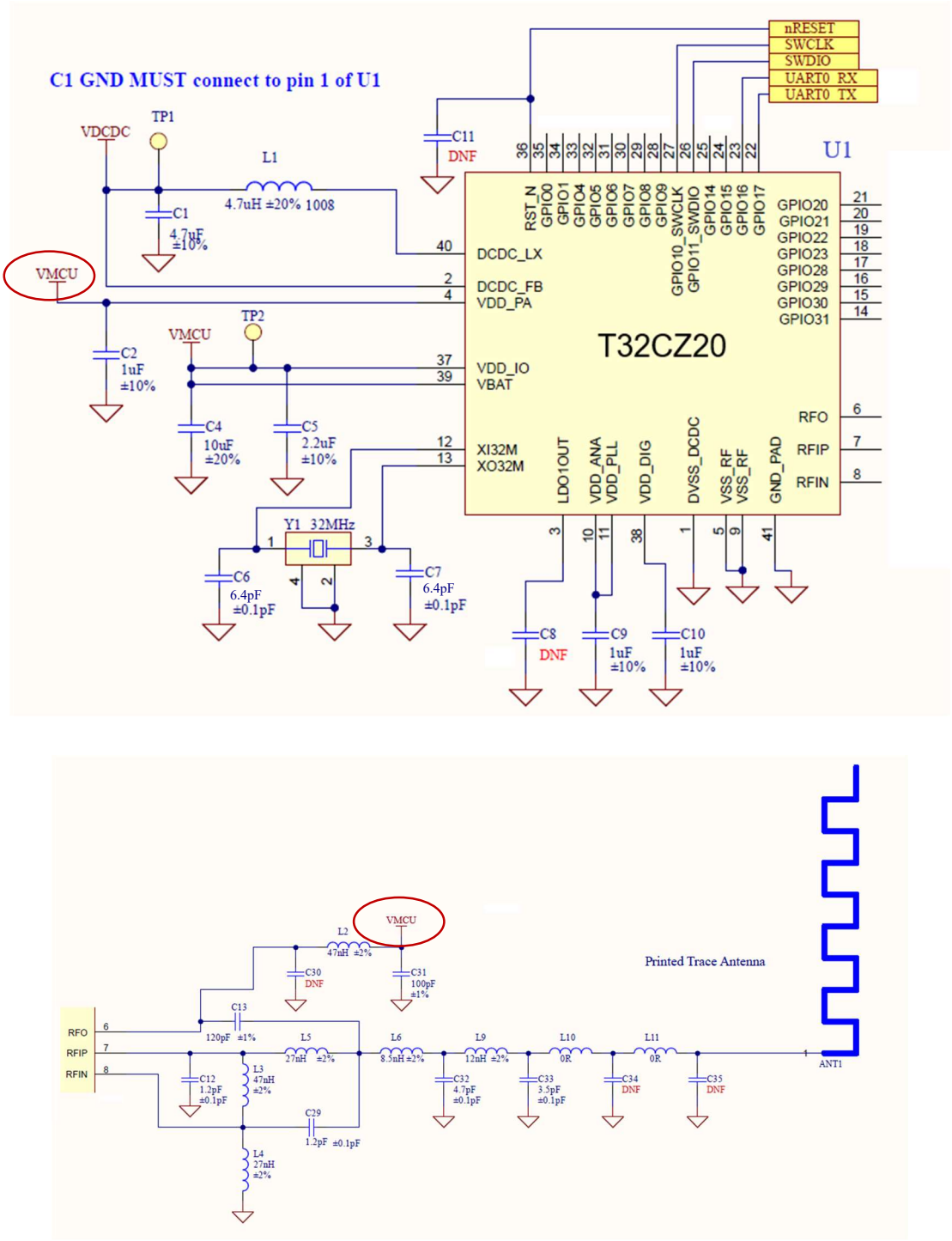


Figure 3.2-1 Application Circuit for +20 dBm Transmit Power

4. Package Specifications

4.1 Package Dimensions

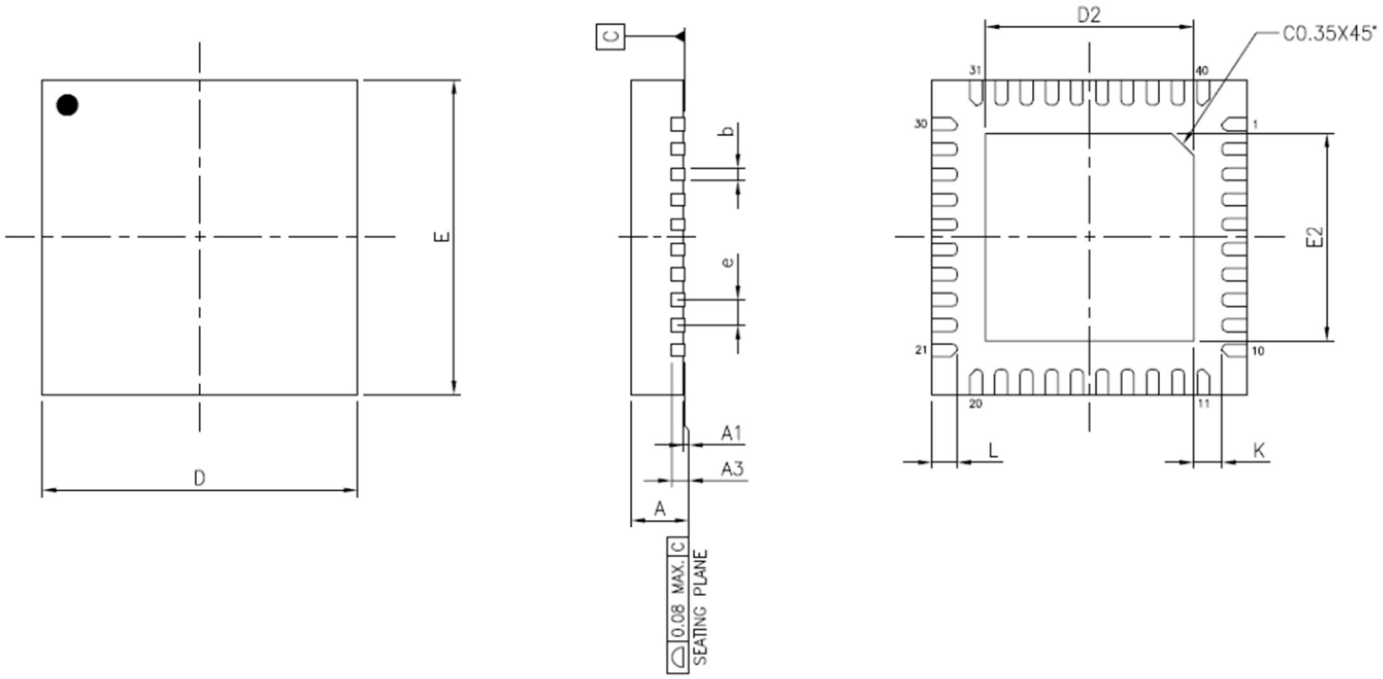


Figure 4.1-1 QFN Package Drawing

	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN 5X5 40L		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	-	-
D2	3.25	3.30	3.35
E2	3.25	3.30	3.35

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

4.2 Manufacturing Guidelines

The following figure 4.2-1 is the recommended soldering reflow profile for the T32CZ20 SOC.

	Ave. Ramp-up Rate	Preheat Time	Peak Temp.	Liquidus Temp.	Time Above Temp.	Ave. Cooling Rate
Scope	217.00 - 260.00 ℃	150.00-200.00 ℃	------	217.00 ℃	255.00 ℃	260.00-217.00 ℃
Condition	0.00 - 3.00 (℃/ sec)	60.00 - 120.00 (sec)	260.00 - 265.00 (℃)	60.00 - 150.00 (sec)	30.00 - 40.00 (sec)	6.00 - 0.00 (℃/ sec)
Sensorl	0.63	85.00	261.70	105.00	32.00	1.68

Figure 4.2-1 SOC Solder Reflow Profile

4.3 Package Marking

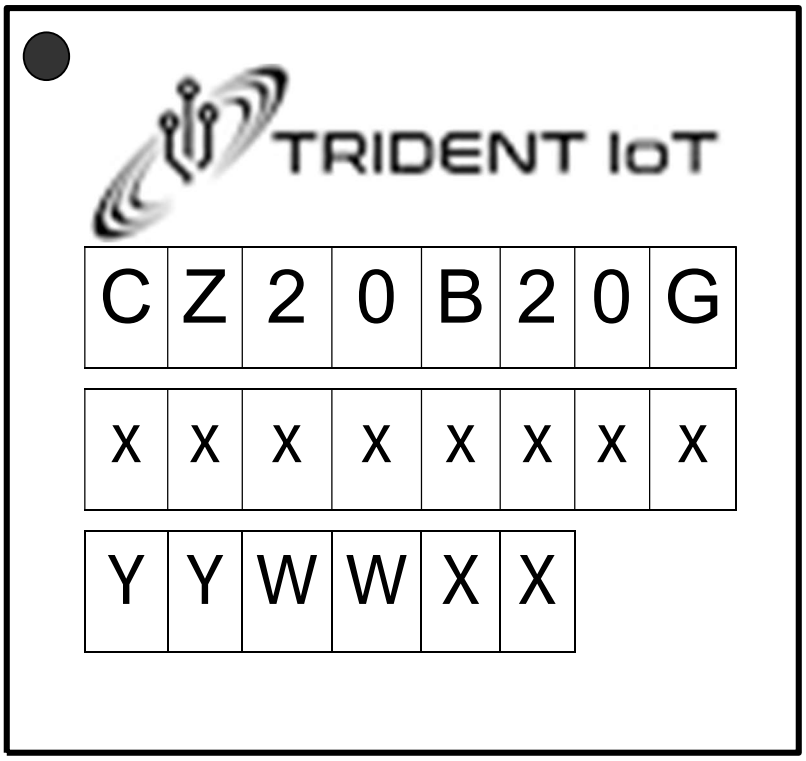


Figure 4.3-1 T32CZ20 Package Marking

Mark Method	Laser	
Font Size	Logo：4.1mm x 1.7mm Device Number：0.45mm x 0.3mm Mfg Code & Date Code：0.45mm x 0.3mm	
Line 1 Marking	Circle = 0.25mm Diameter (Top-left justified)	Pin 1 identifier
Line 2 Marking	Device Number	CZ20B20G
Line 3 Marking	XXXXXXXX = Mfg. Code	Manufacturing code varies by batch.
Line 4 Marking	YYWWXX YY = Year; WW = Work Week XX = Control Code	Year & work week of the mold date. Trident IoT internal control code

5. Development Support

5.1 Developer Tools and SDK

Name	Description	Features
ELCap	ELCap is Trident IoT's Cross-Platform Command Line based development tool. This is the starting point from which to manage all device Trident SDKs. Develop, compile and flash all your Trident SoC based applications from one easy to use application.	• Command Line Interface • Enables and Orchestrates the containerized build environment within Trident SDK • VS Code Extension
Trident SDK	Software development kit for Z-Wave and Zigbee device applications using Trident IoT silicon.	• Patented Remote Command Line Interface • In-field upgrades • Bootloader • Secure boot • Signed upgrade images • FreeRTOS based applications • GCC (The GNU Complier Collection) • Integrated Build Environment.

5.2 Evaluation and Development Hardware

Part Number	Description	Features
DKN-CZ20B20-02	CZ20 Evaluation Board	• Integrated J-Link OB programmer & debugger • Power Supply: USB-C, CR2450 powered, ext pwr • Connectors: QWIIC, ADR Maker Shield • On Board Buttons (3), RGB Led (1) • PCB Trace Antenna
DKR-HOST-00	Main Development Board used for development and factory programming	• Integrated J-Link OB programmer & debugger • Power Supply: USB-C, CR2450 powered, ext pwr • Connectors: Radio Board Connector, QWIIC, ADR Maker Shield, Full I/O breakout for Target chip • On Board Buttons (4), LED (4)
DKR-CZ20B20-25	CZ20 Radio Board used for development, factory testing, and RF evaluation.	• Power Supply: via DKR-HOST-00 • Connectors: Radio Board Connector to DKR-HOST-00 • Selectable Antenna via solder bridge: PCB Trace Antenna or 50 ohm SMA connection • Selectable TX PWR via solder bridge: 14 or 20 dBm • Footprint for External Flash

5.3 Hardware Guides

Documentation regarding implementation and validation of the T32CZ20:

Document Number	Description	Features
HG-ZW-0001	Hardware Implementation Guide	• PCB Layout guidelines • Programming Footprint Reference • RF Matching, RF Calibration, TX Power Application Circuits
HG-ZW-0002	Hardware Bring Up Guide	• Hardware Design Considerations for Bring Up • Guidelines on Testing RF Performance • Guidelines on testing Electrical Performance • Guidelines on Reliability Testing

6. T32CZ20 Revision History

Revision	Date	Description
A	10/28/2025	Release

7. Datasheet Revision History

Revision	Date	Description
-02	October 28th, 2025	• GA release Updates • Updated language • Removed Deep-power down modes • Updated Names of BOD & AUX comparator to Brown-Out Detector and Analog • Added Solder Reflow profile • Updated Figure & Table numbers to match corresponding section
-01	March 31, 2025	• Beta Release

8. Contact Us

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8.1 Support

Informational Links	
Support Documents	https://tridentiot.com/products/
SDK Manuals	https://tridentiot.github.io/tridentiot-sdk-docs/
Hardware Documents	https://tridentiot.com/technology/hardware/